



Small Talk 2024

EUV Products and Business opportunity

Peter Vanoppen

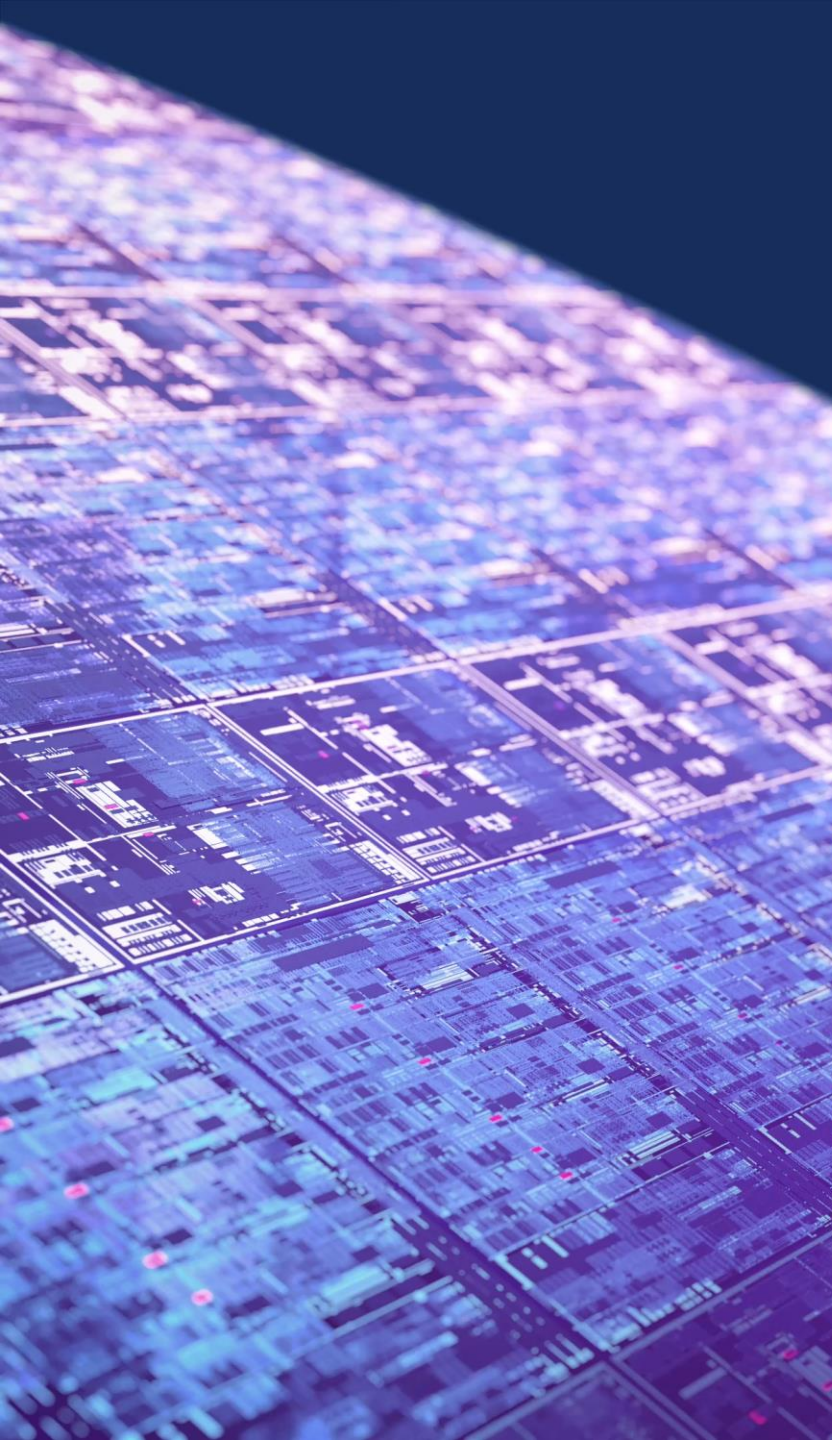
Executive Vice President and Head of Business Line 0.55 NA EUV

Teun van Gogh

Executive Vice President and Head of Business Line 0.33 NA EUV

ASML Investor Day

Veldhoven, The Netherlands
November 14, 2024

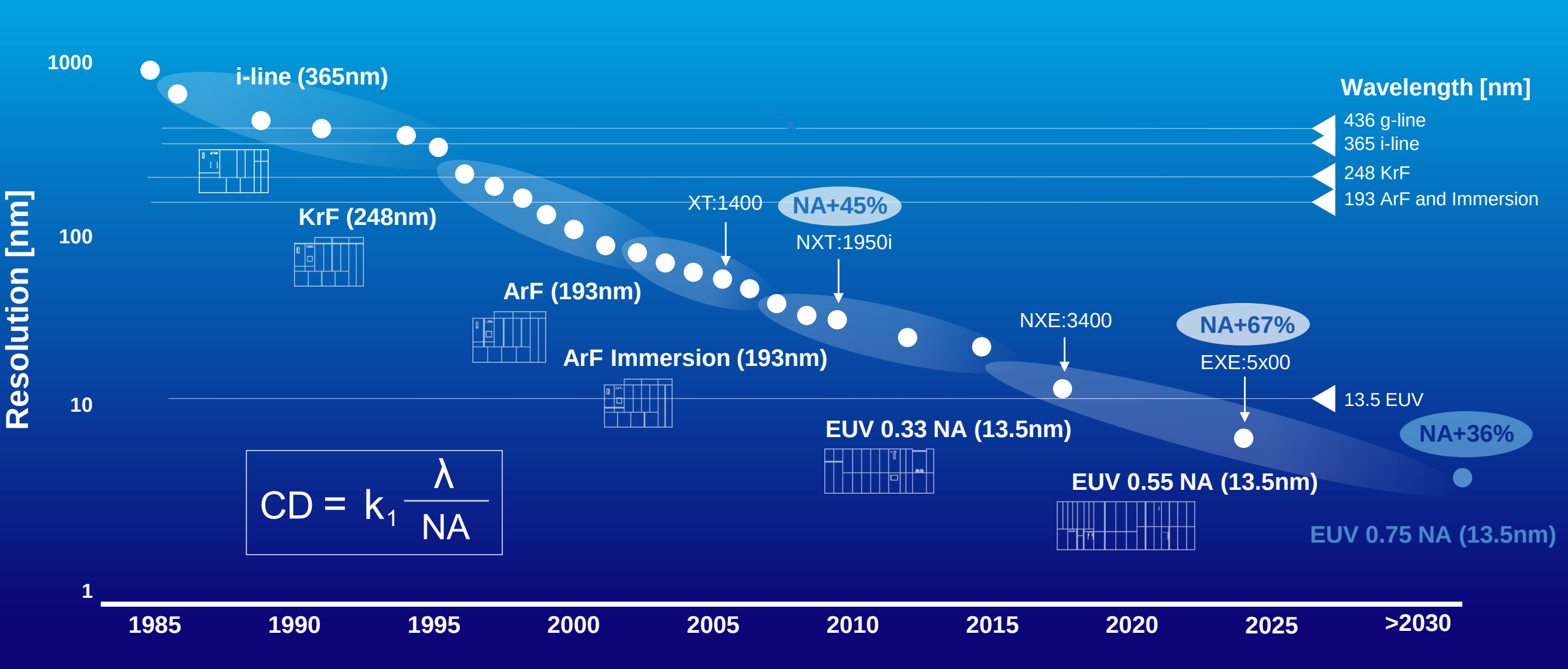


Key messages

- EUV has reached **high-volume manufacturing maturity** providing a solid foundation for continued innovation.
- The **NXE:3800E** offers a 38% improvement in productivity and 13% in overlay, with additional productivity and overlay improvements planned for the NXE:4000F and beyond.
- The **imec ASML High NA EUV lab** opened in June, and all EUV customers have exposed critical layers. The data prove the capability of the system in **lowering costs by 20-35% for critical layers** compared to 0.33 NA, by dose reduction, enabling single exposure and 2D layout designs.
- The first **High NA EUV systems** are operational at a customer, marking a key milestone in adoption of High NA EUV.
- In the future both 0.33 NA and 0.55 NA EUV systems will be used for critical exposures. The **EUV roadmap for the next decade** includes the introduction of a high productivity platform and will enable **affordable scaling** for both 0.33 NA, 0.55 NA and potentially Hyper NA.
- The growing **installed base opportunity** will be leveraged with a value-based service model in combination with productivity and performance upgrades.

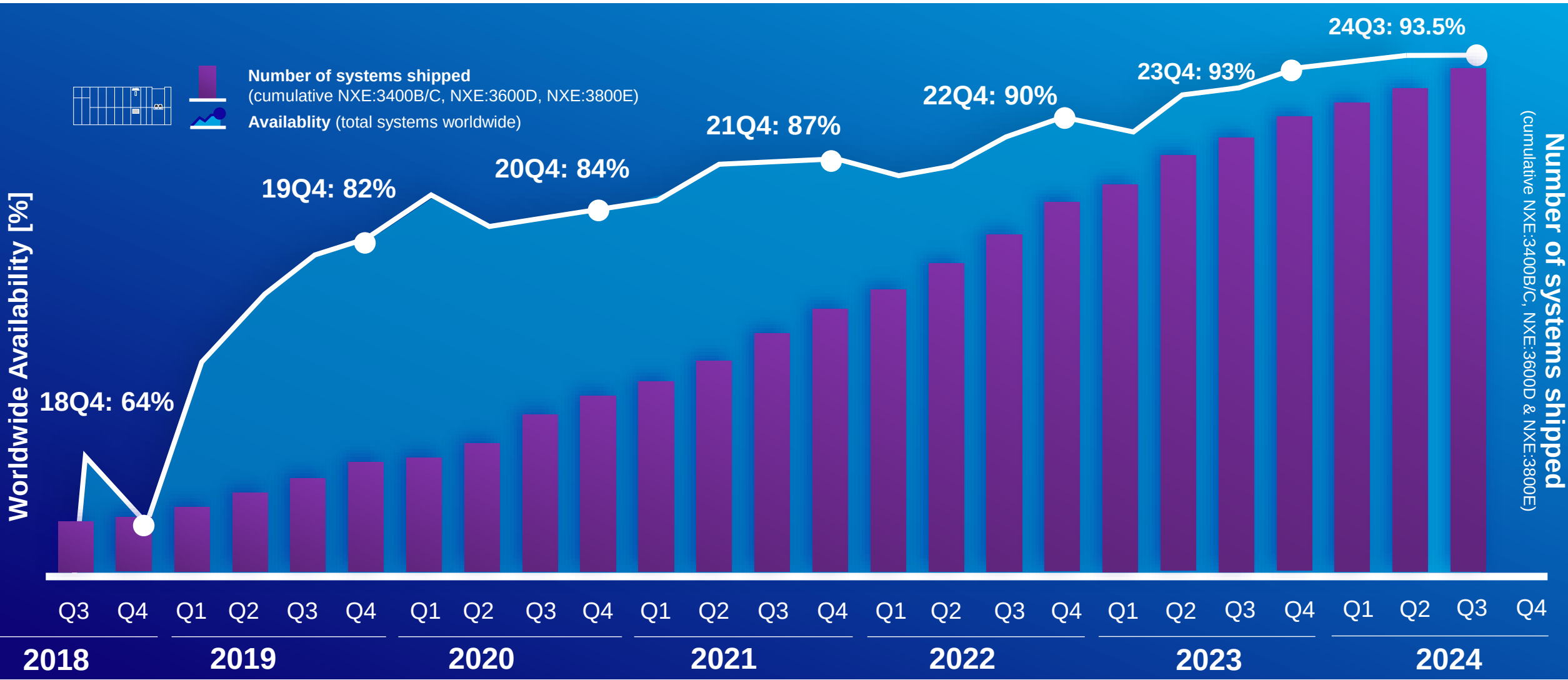
EUV lithography enabling a resolution improvement of 2 orders of magnitude

to enable the most advanced chip manufacturing



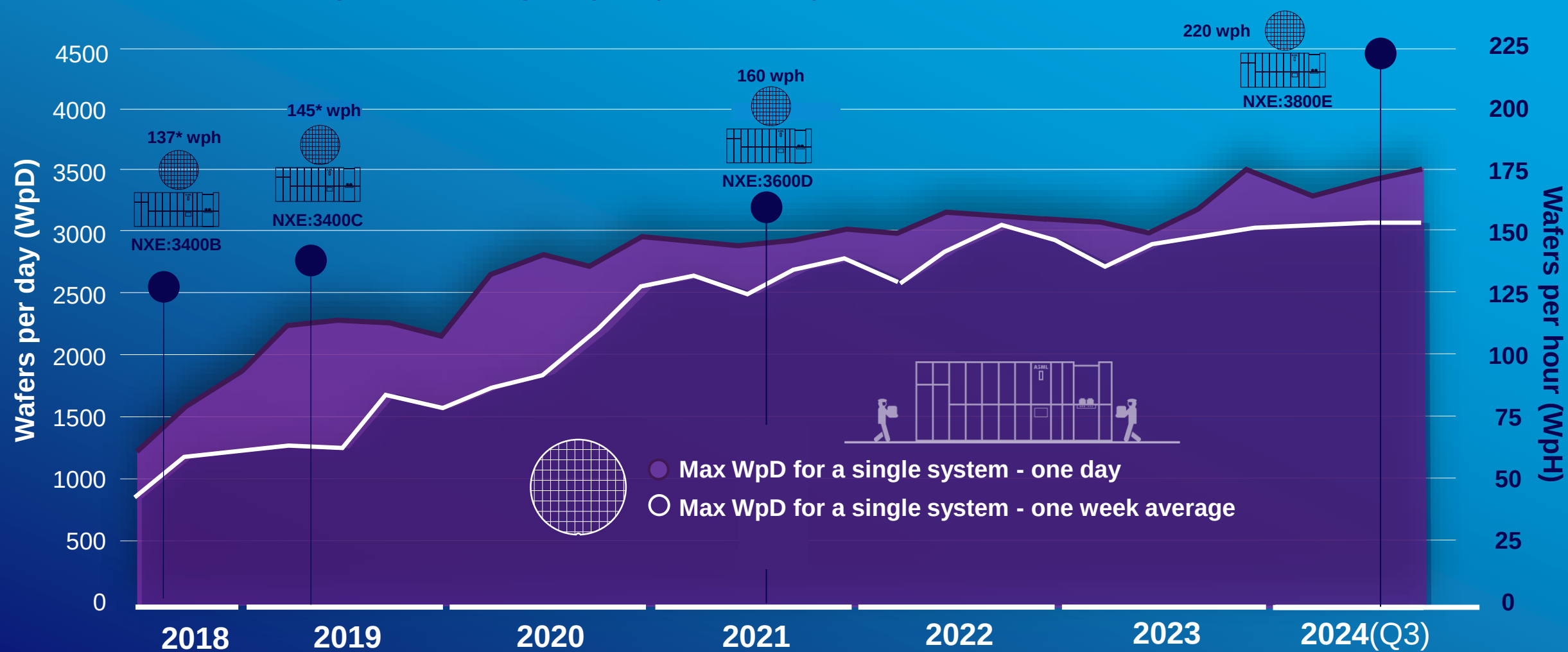
0.33 NA EUV systems exceeding 93.5% worldwide average availability (Q3 2024)

Moving towards 95% worldwide availability



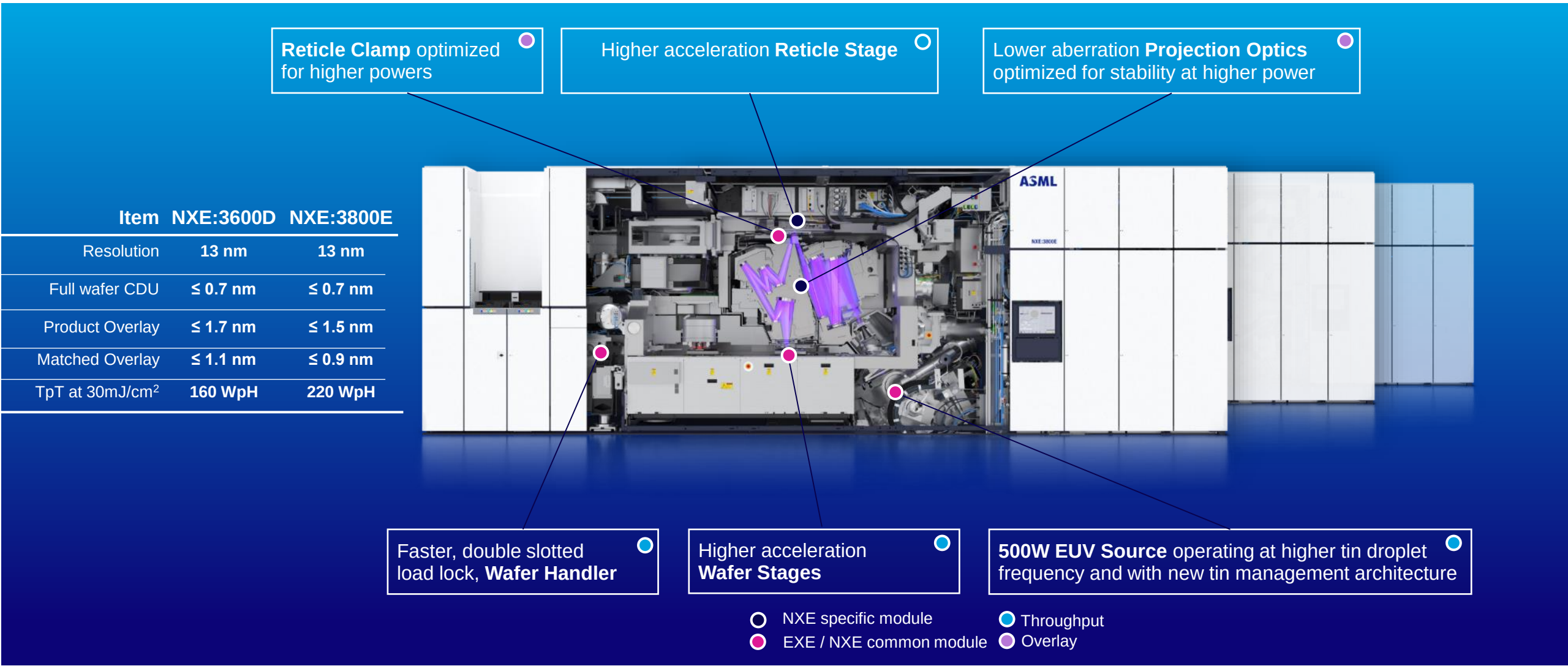
NXE productivity steadily increasing over the years

NXE:3800E enabling the next big step in productivity for our customers



* including Productivity Enhancement Package (PEP)

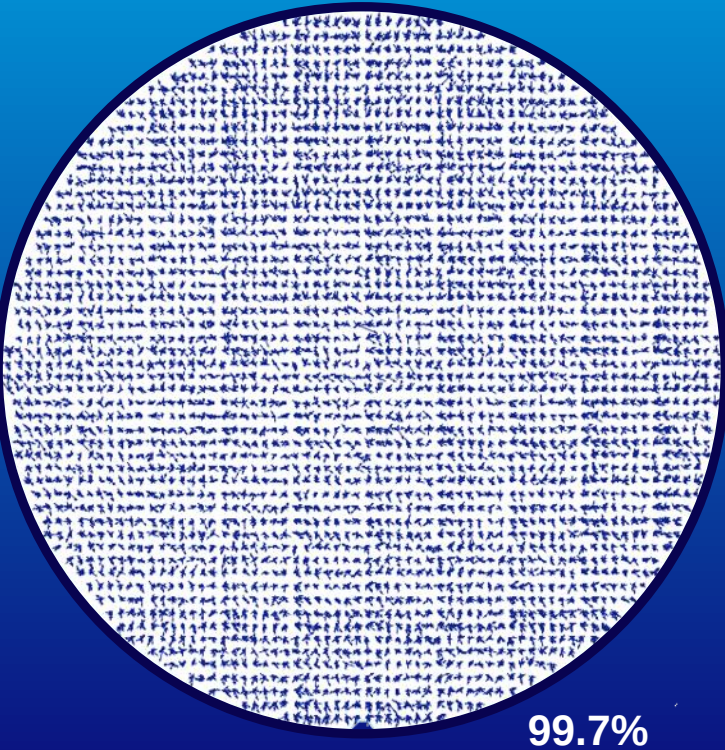
NXE:3800E improves productivity from 160 to 220 WpH (+38%) and overlay by 13% to enable EUV on 2 nm node



NXE:3800E – Dedicated chuck overlay 0.6 nm at 220 WpH, with spec at 0.8 nm

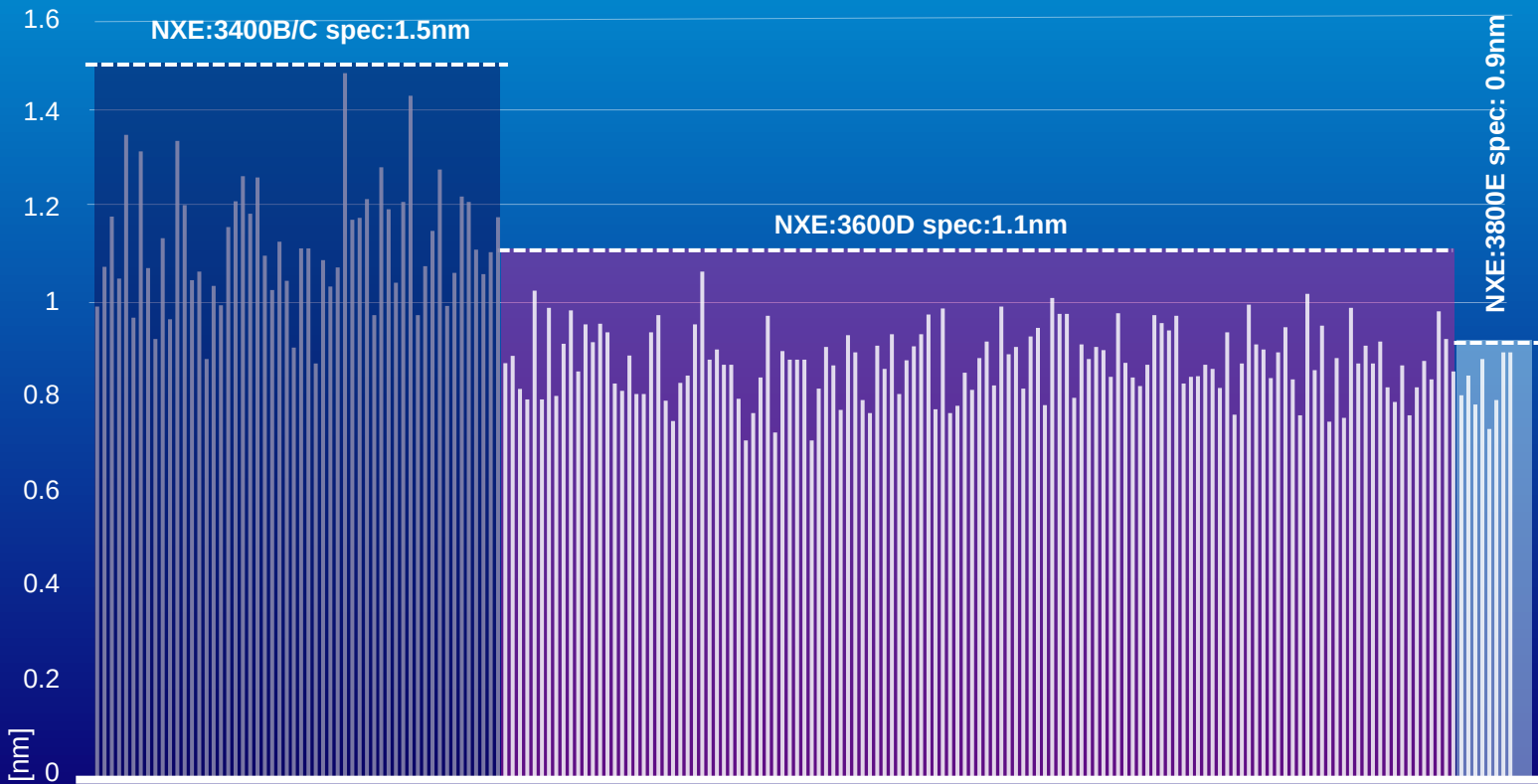
Matched Machine Overlay shows expected performance improvement

Dedicated Chuck Overlay at 220 WpH



Overlay X: 0.5 nm
Overlay Y: 0.6 nm

Matched Machine Overlay population at 195 WpH:
NXE:3400C, NXE:3600D, NXE:3800E



Each bar represents a system qualification at ASML factory

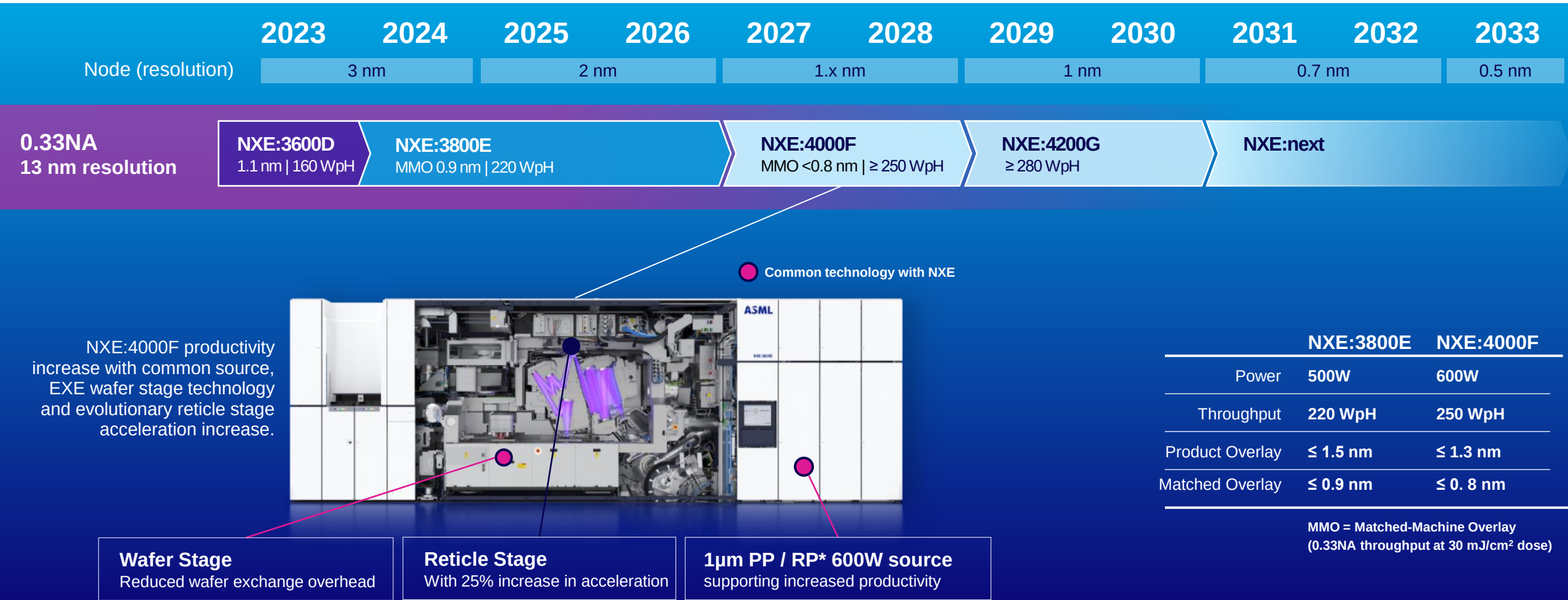
EUV customers are installing NXE:3800E at their R&D and HVM sites from 2024

NXE:3800 installed at DRAM, LOGIC and Foundry customers



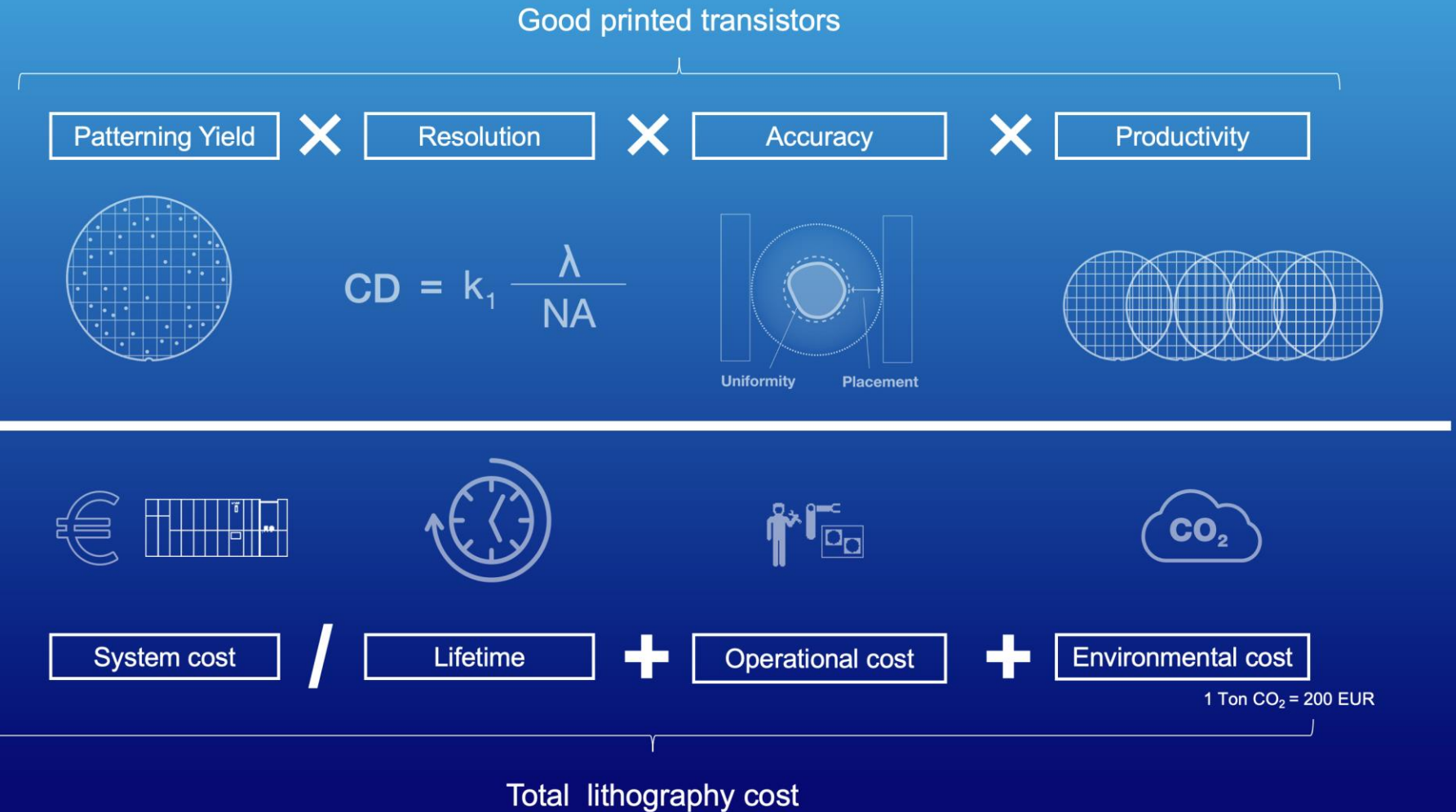
NXE:4000F specified at ≥ 250 WpH and 0.8 nm Matched Machine Overlay

Enables improvements in both productivity (14%) and overlay to enable 0.33 NA EUV on the 1.4 nm node

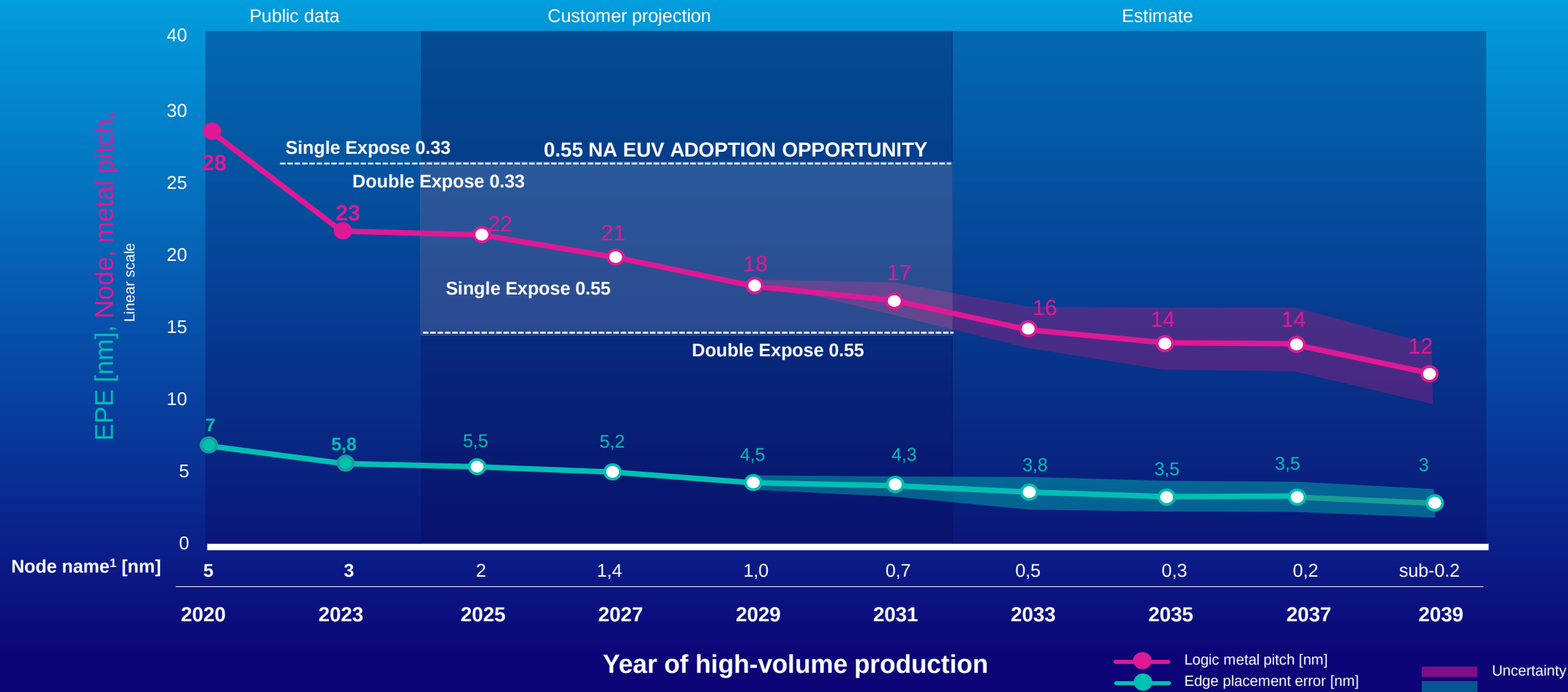


ASML will innovate in EUV to lower the cost of good printed transistors

Our portfolio with 0.33 NA, 0.55 NA and potentially Hyper NA will provide full flexibility to our customers



High NA EUV opportunity starts now as 0.33 NA EUV transitions to multi-patterning on <26nm pitch critical layers



High NA EUV – Introducing high-resolution, high-contrast imaging technology

The latest addition to ASML’s holistic lithography roadmap

High NA EUV Lithography

Patterning Yield

- Process simplification
- Increased design flexibility, 2D patterns

Resolution

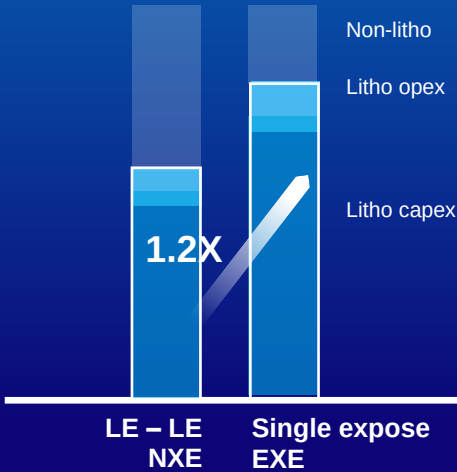
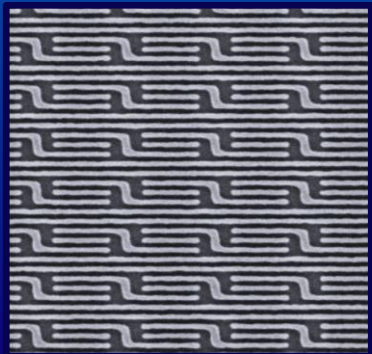
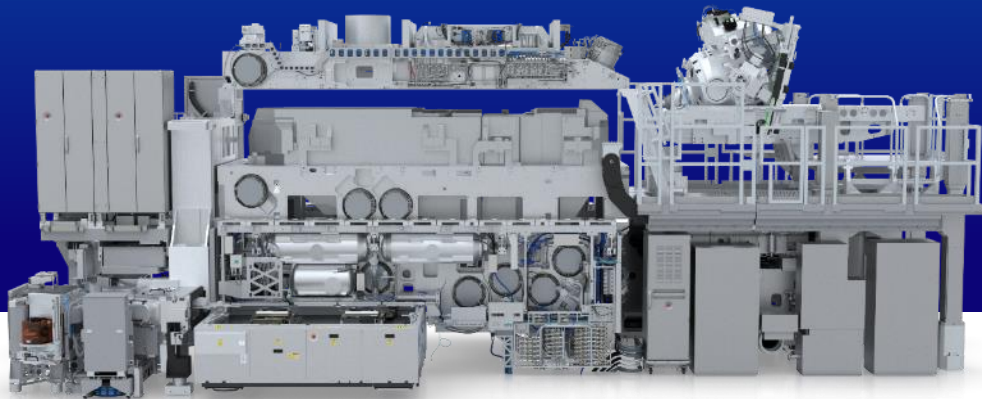
- High contrast
- 2.8x improvements in density

Accuracy

- Best-in-class overlay performance
- High-contrast imaging for LCDU gain

Productivity

- Single expose vs. multi-patterning
- High contrast imaging for lower dose



Legend: LE = Litho-Etch

High NA EUV technical values and customer benefits

High NA technical values



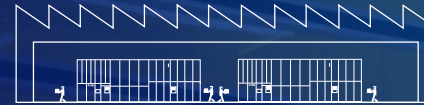
**0.55 NA higher resolution enables
1.7x smaller features
and 2.8x increased density**



**Higher imaging contrast enables 40%
improvement in Local CDU**
1.4x reduced pattern variability at 1.4x lower dose



Customer benefits



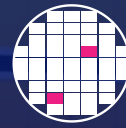
Patterning cost reduction by

- 1) Enabling single patterning (from multi patterning)
- 2) Dose reduction with higher contrast (productivity)
- 3) Enabling 2D designs (device cell shrink)



Reduced defect density by

- Process simplification, improved edge placement error
- Less mask = less patterning process defects



Shorter cycle time

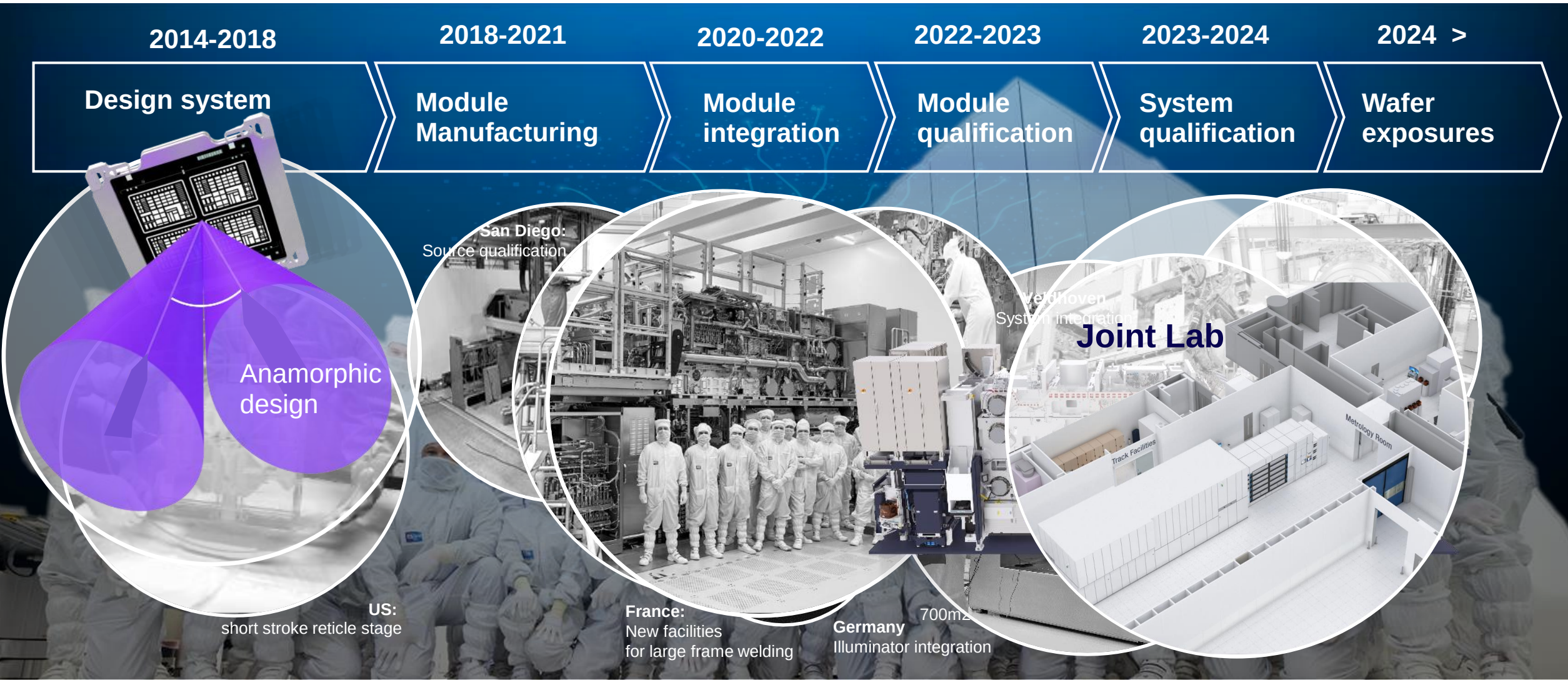
- 1-2 days saved per mask reduction

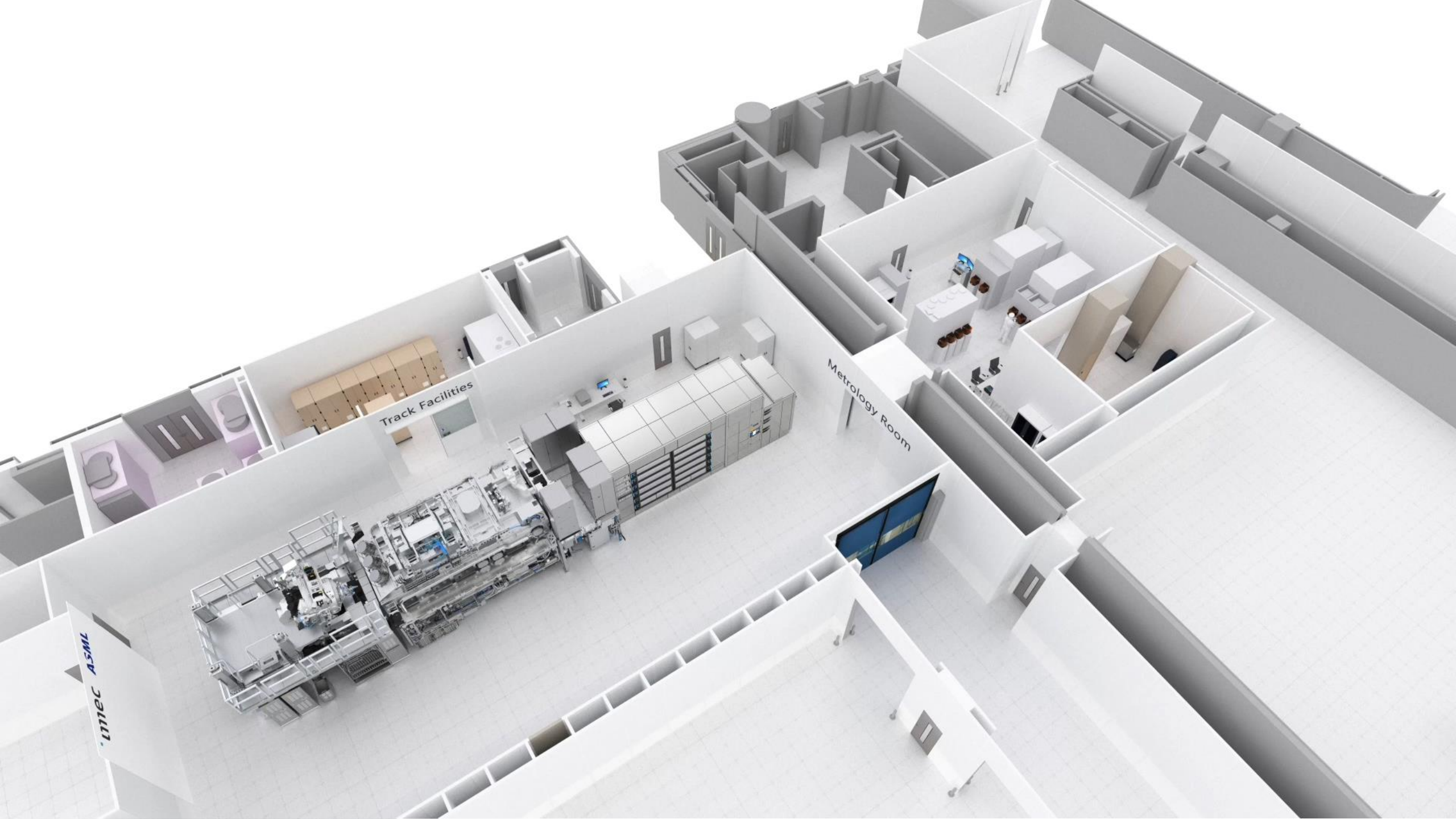


Less patterning fab space



A decade of development leading to the opening of the joint imec ASML Lab in June 2024





Track Facilities

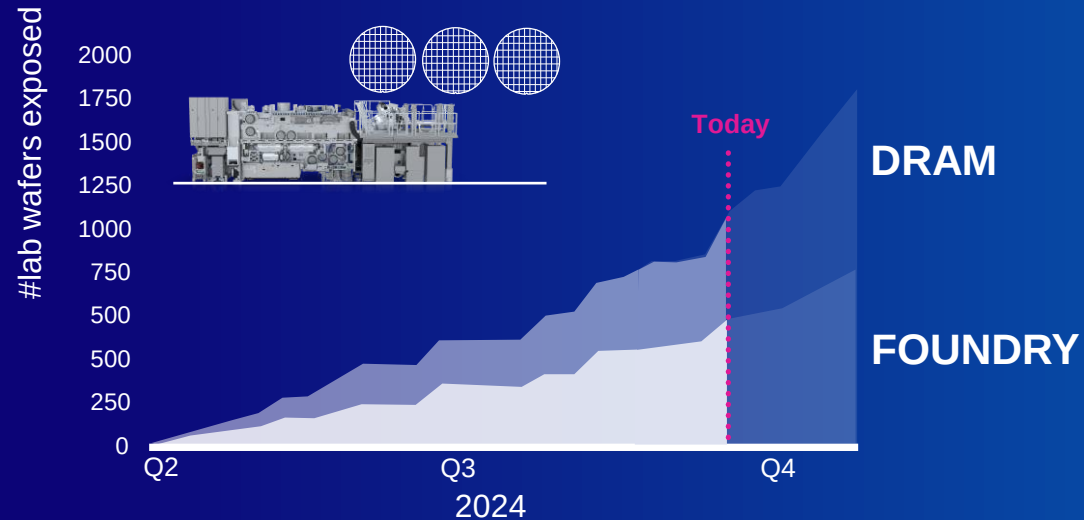
Metrology Room

imec ASML

Customers have exposed critical layers in High NA EUV lab & verified the benefits

Progress on High NA recognized and its importance in enabling cost effective scaling acknowledged

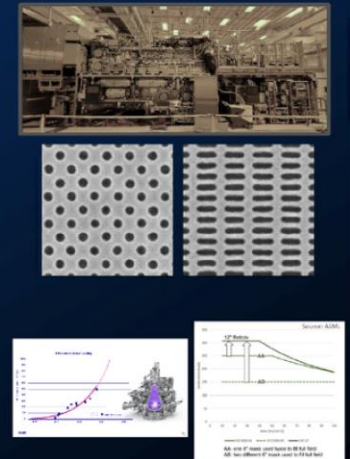
In total >10,000 wafers exposed on the high NA systems including >1300 DRAM and Foundry customer wafers in the lab, expecting to reach ~2000 wafers by the end of the year



Mark Philips (Intel) reports on High NA at SPIE photomask technology, September 2024

Executive Summary

- High NA EUV is here: healthy tools, available in the field, with a full suite of holistic applications
- The ecosystem is ready to support process development: reticles, resists, underlayers, etches, OPC and metrology
- The expected benefits of higher NA are evident in resist images
- There are devices (RibbonFETs) and interconnects (enabled by PowerVia) ready to take advantage of the higher resolution
- The timing is right to avoid the cost and complexity of excessive mask splits with 0.33NA EUV
- "6x12" masks will enable 23-50% productivity improvement on the EXE:5600, and potentially more on future platforms



Logic Technology Development

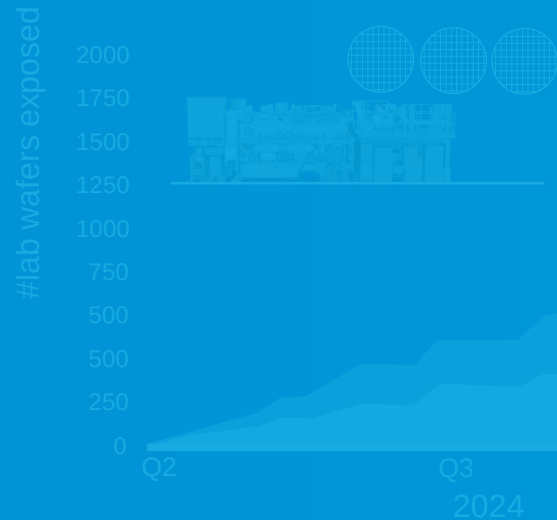
SPIE Photomask Technology + EUV Lithography, 30 September 2024 - Mark Philips

intel foundry

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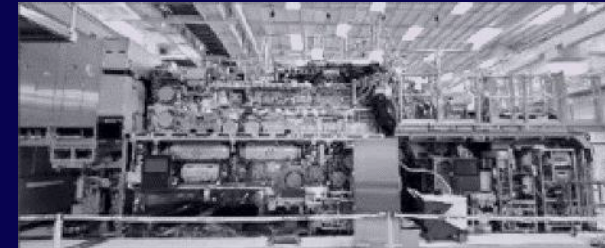
In total >10,000 wafers exposed on the High NA EUV lab, including >1300 DRAM and Foundry customers, with more expected to reach ~2000 wafers by the end of 2024.



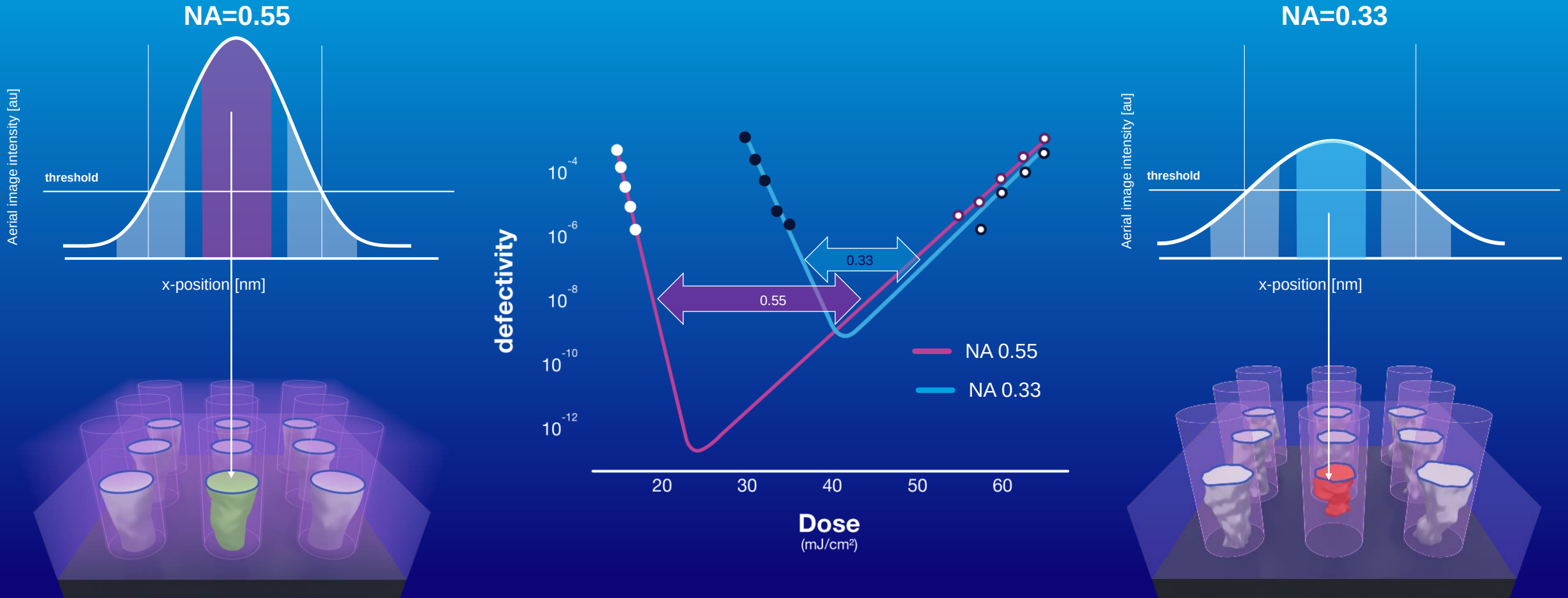
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Mark Philips

intel foundry



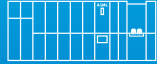
High NA EUV high-contrast imaging increases process window while reducing dose requirements and patterning defects resulting in higher productivity and better yield



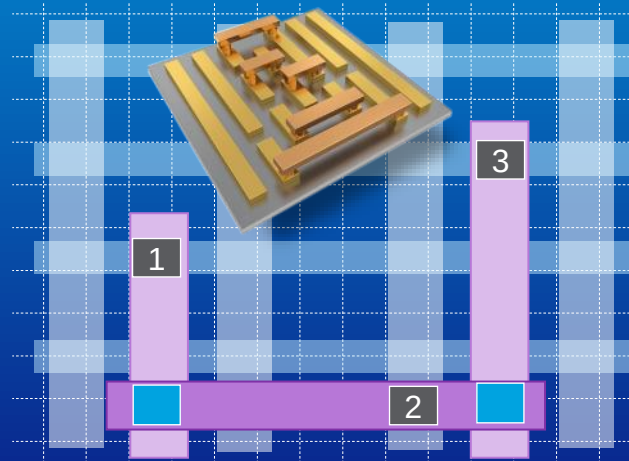
High NA EUV offers a new design opportunity going for 2D design layouts

This enables higher logic cell density (hence scaling) and optimized routing of interconnect layers reducing the total number of metal layers

0.33 NA



Two metal layers (1D) and additional Via layer required to connect 3 transistors

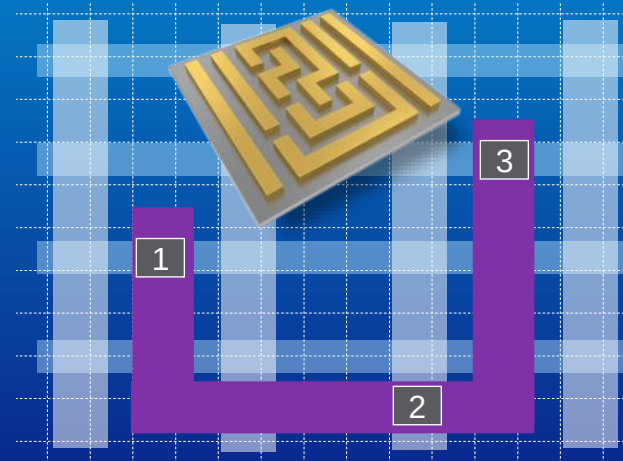


- 1 Contact to transistor
- Metal 1 Vertical
- Via
- Metal 2 horizontal

0.55 NA



0.55 NA resolution and contrast enables single expose of 2D metal, replacing two metal and one via layers



- 1 Contact to transistor
- 2D Metal

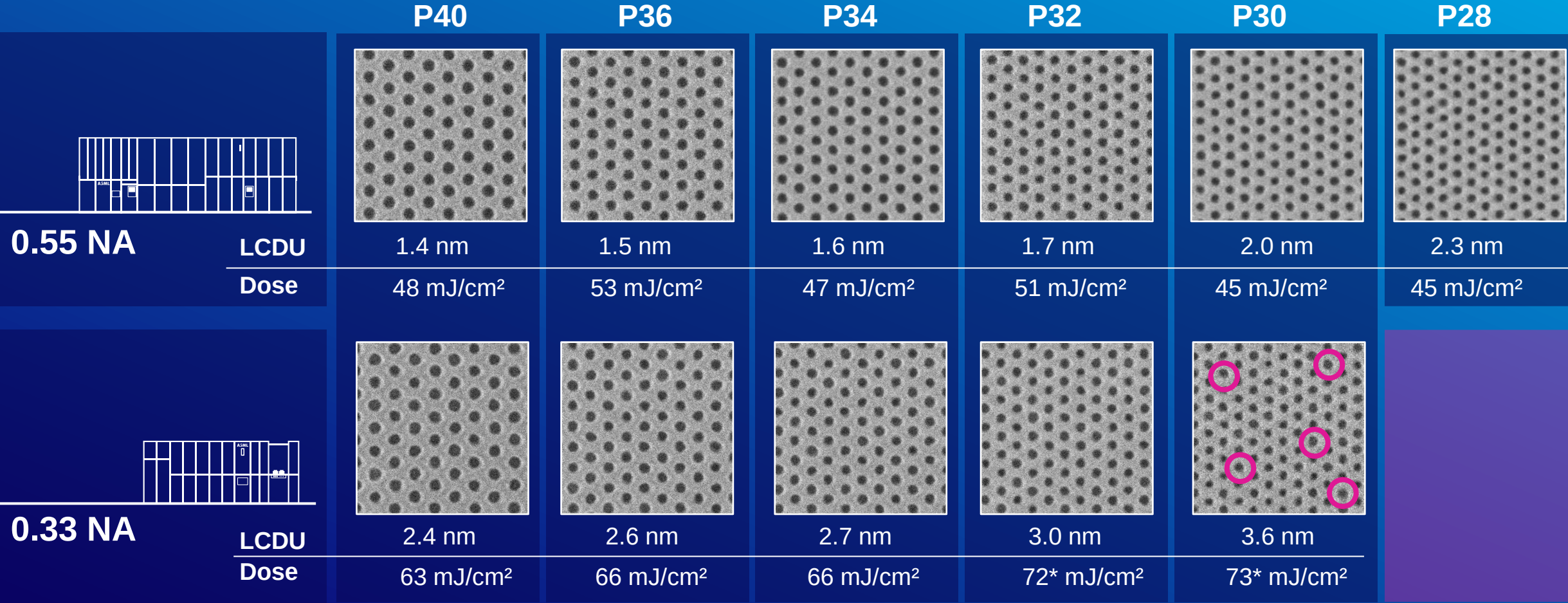
0.55 NA single expose image



P22 in horizontal direction combined with P28 in vertical direction

High NA EUV exposures on contact hole patterns (DRAM layer) through pitch

show higher contrast, resulting in improved LCDU and reduced dose

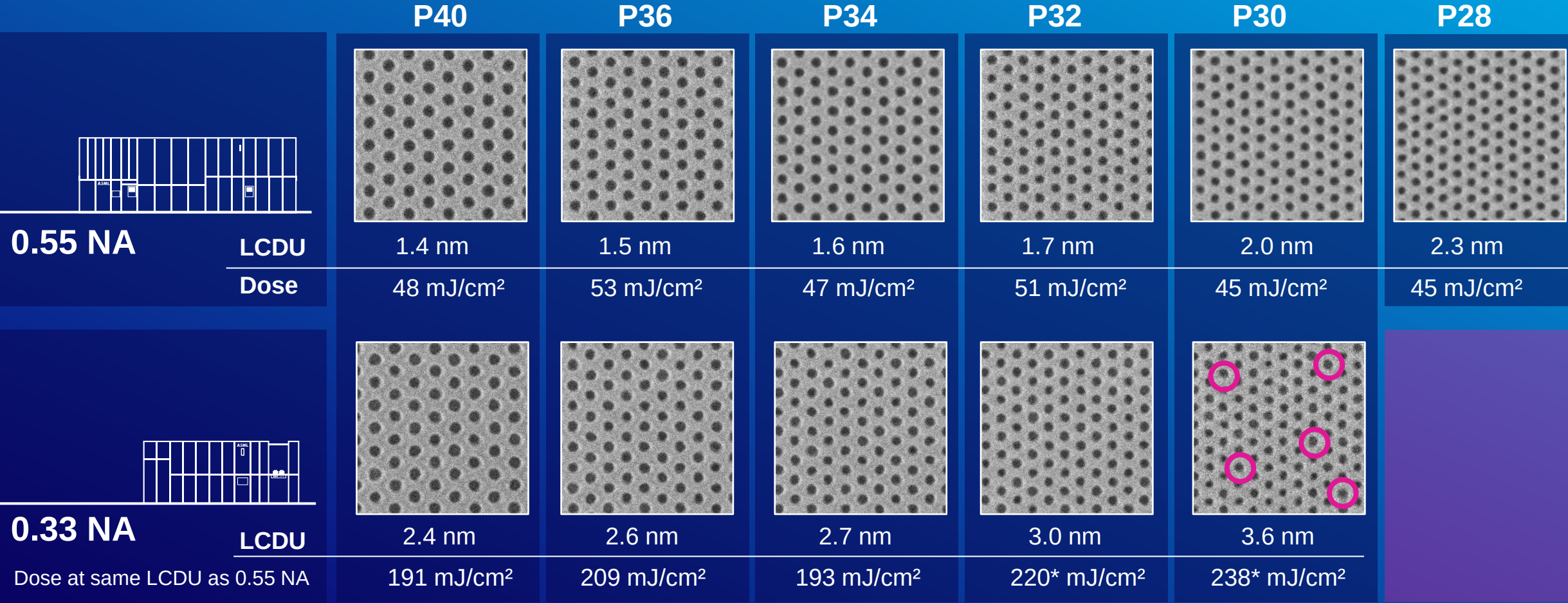


Based on 40nm CAR

*23% illuminator efficiency

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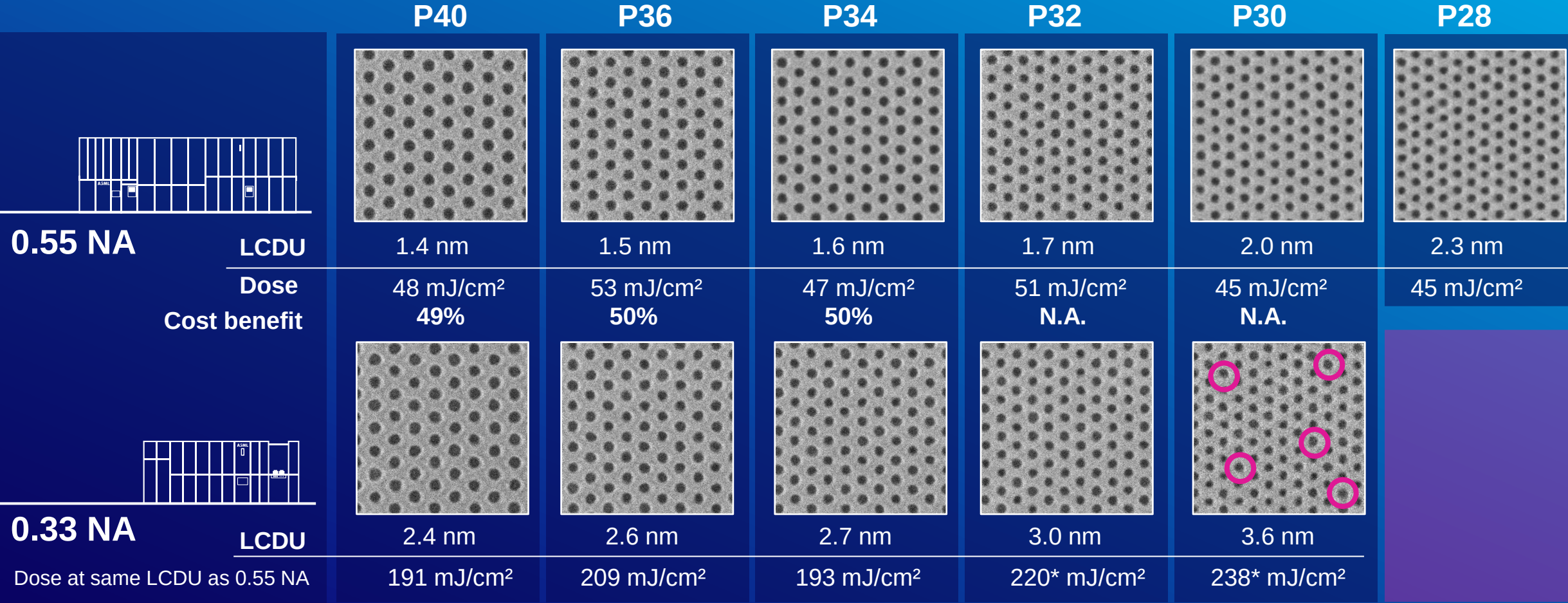


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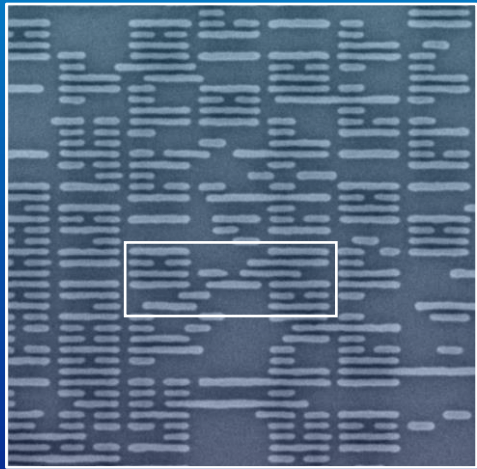


Based on 40nm CAR

The cost benefit of high NA is 50% compared to a low NA exposure at the same LCDU

*23% illuminator efficiency

LOGIC [P19]: High NA EUV single exposure will enable ~35% cost benefit and significant process simplification compared to multi patterning 0.33 NA EUV



P19 T2T ~15 nm | After etch

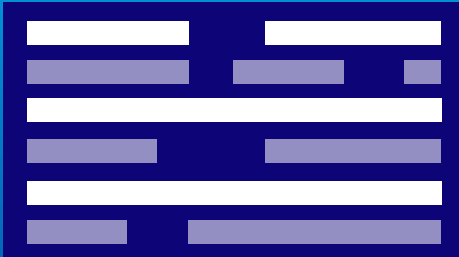
0.33 NA
Multi Patterning

Exposure 0.33 NA ①



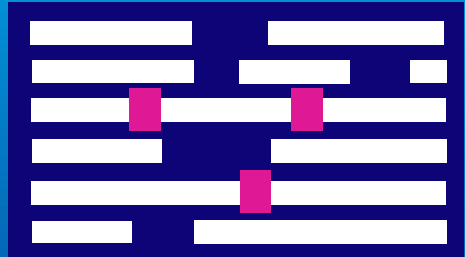
Litho etch

Exposure 0.33 NA ②



Litho etch

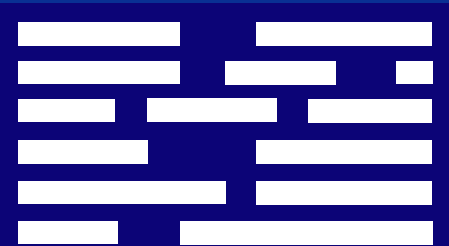
Exposure 0.33 NA ③



Cut

0.55 NA
Single Patterning

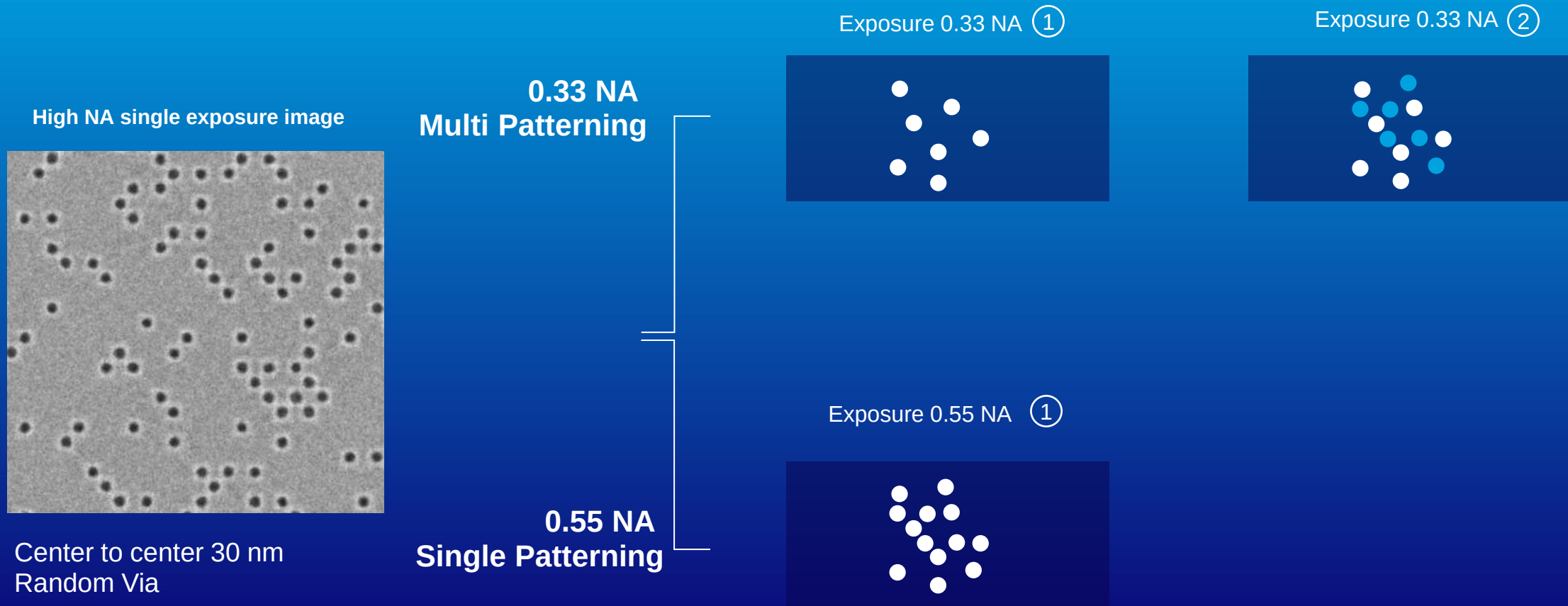
Exposure 0.55 NA ①



Litho etch

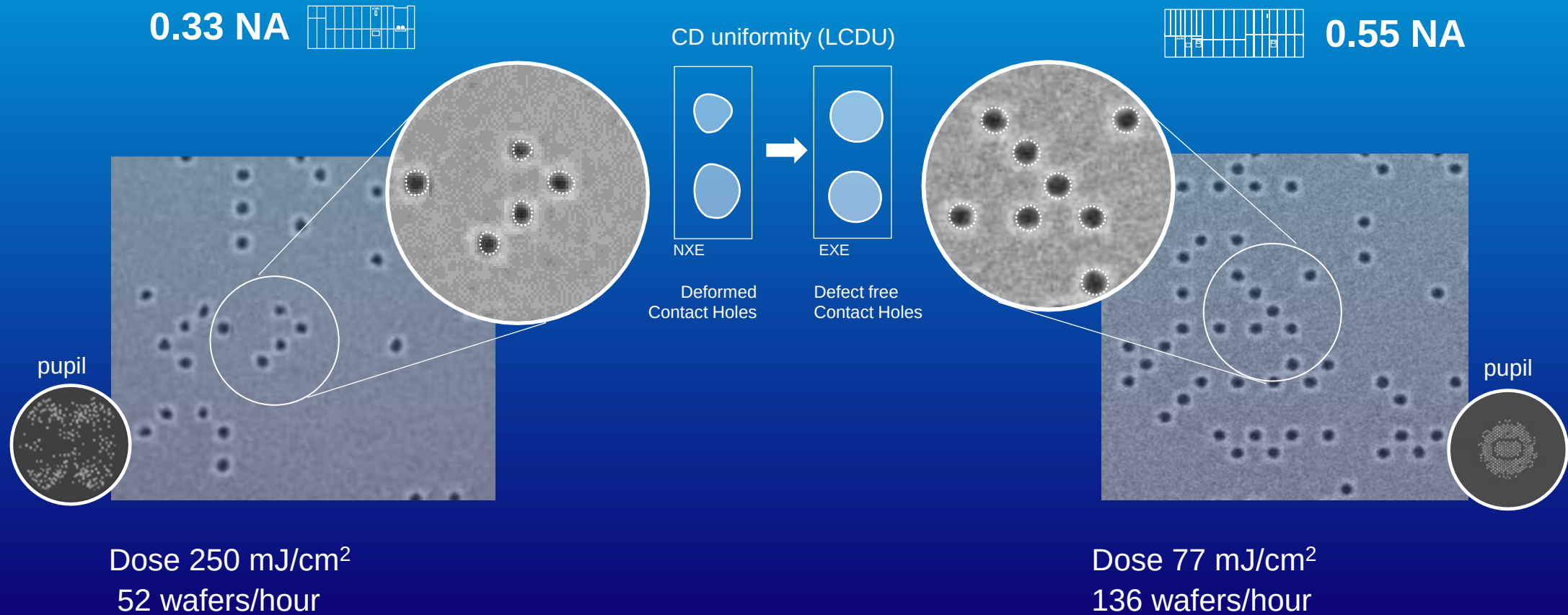
LOGIC [P30]: ~20% cost benefit and process simplification

moving from double exposure 0.33 NA EUV to single exposure High NA EUV



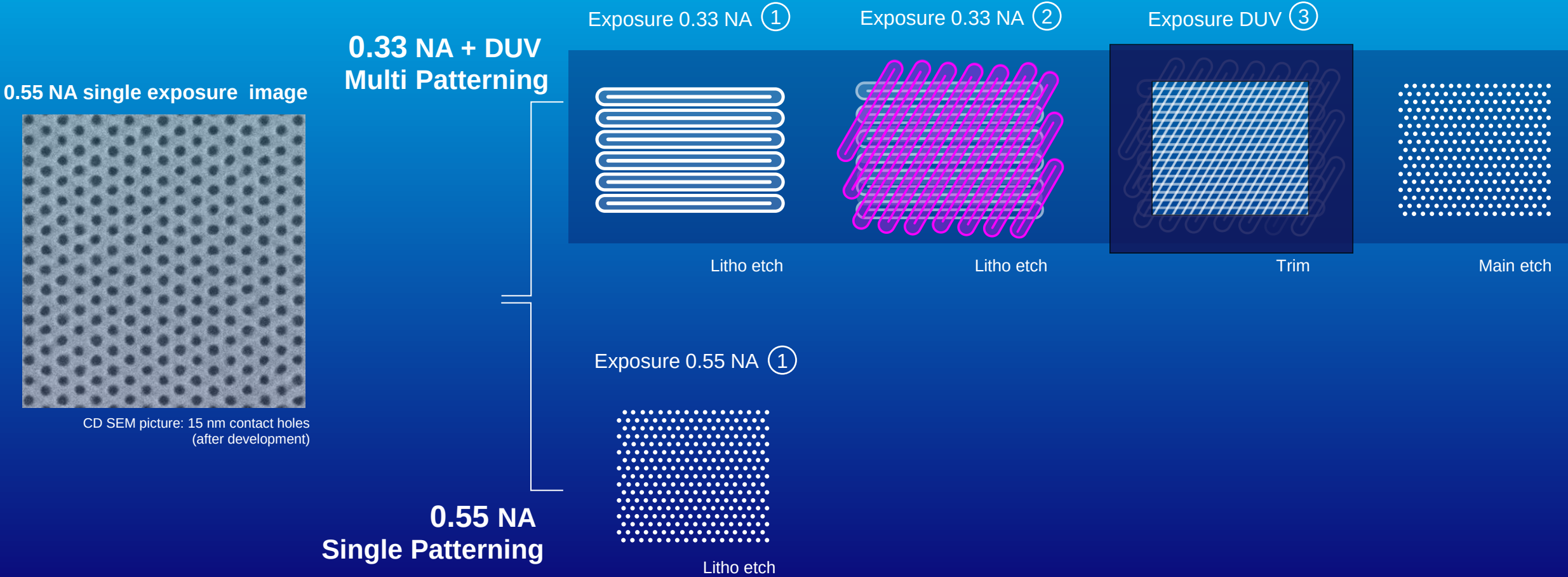
LOGIC [P36]: Higher contrast enables lower exposure dose at better imaging quality resulting in higher productivity and lower cost

Single exposure comparison (Logic Via layer, 18 nm holes, pitch 36 nm)



DRAM 15nm contact holes: High NA enables high productivity single exposure

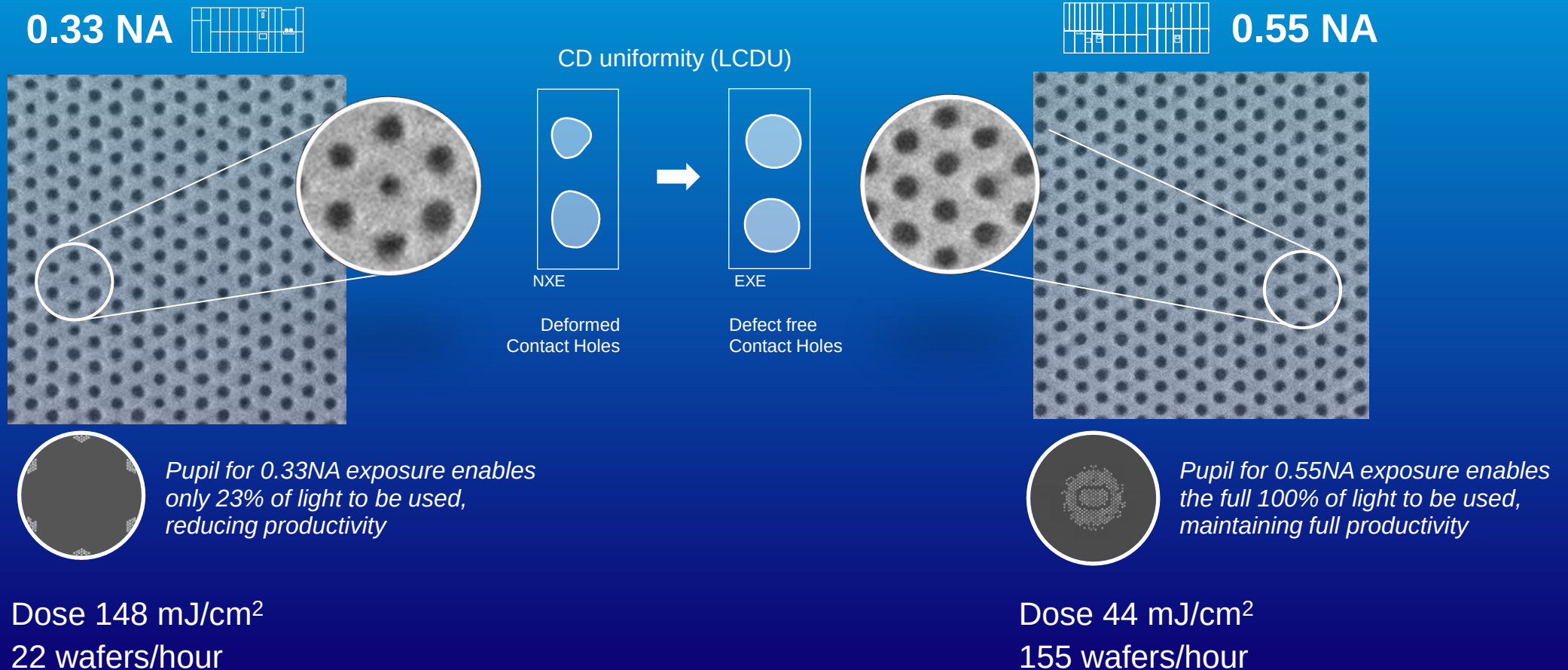
Moving from triple exposure (2x 0.33NA EUV +1x DUV) to single exposure 0.55 NA EUV



High NA DRAM Capacitor: ~30% cost benefit and process simplification

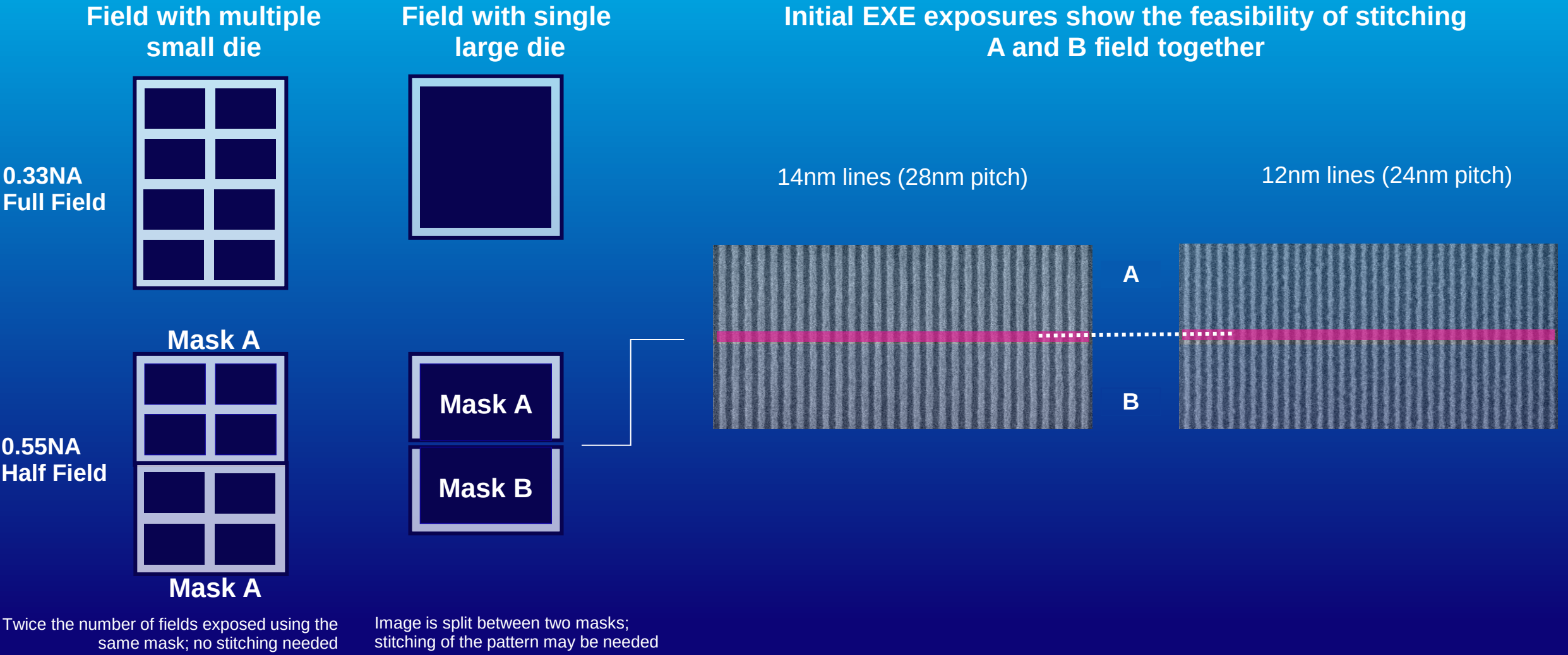
DRAM 15 nm contact holes: Higher contrast of High NA enables lower exposure dose at better imaging quality, resulting in higher productivity and lower cost

Single exposure comparison (DRAM capacitor layer, 15 nm holes)



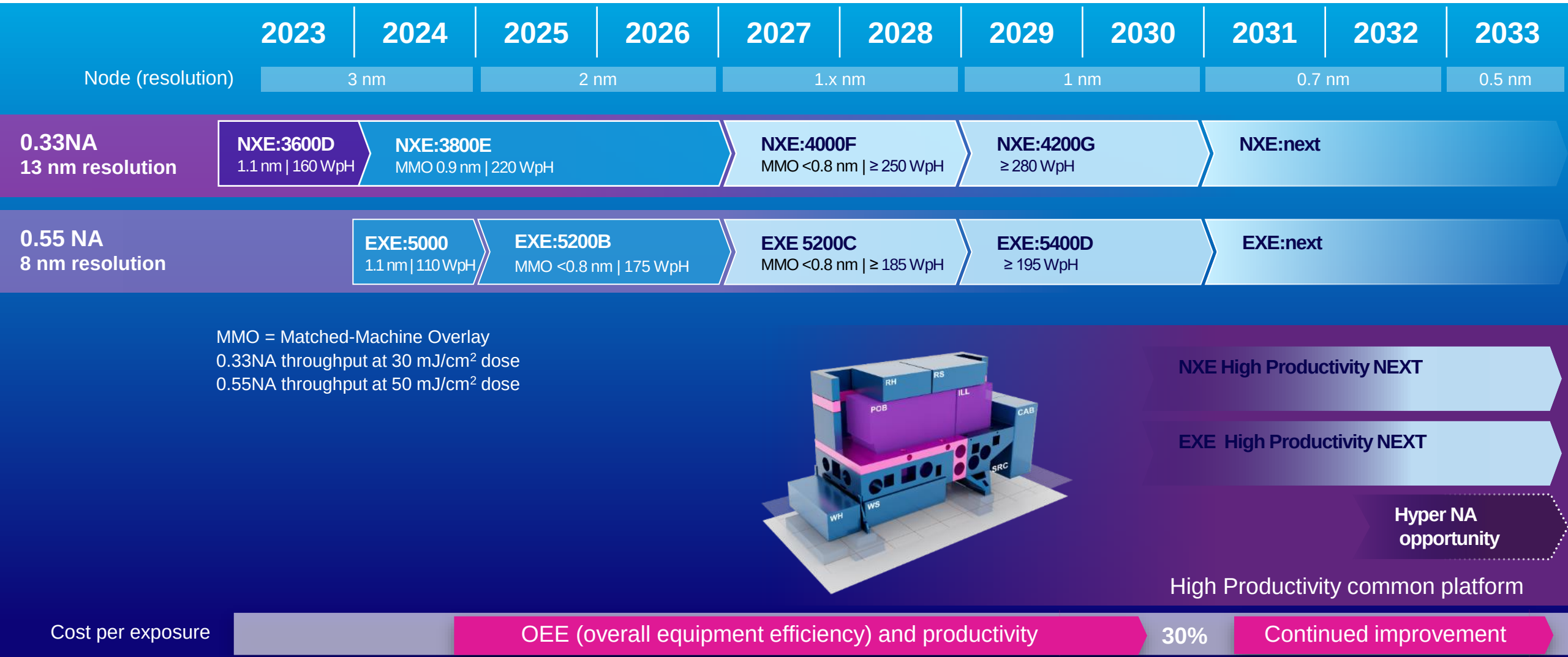
High NA half field exposure requires stitching for large die

Engineering solutions available to enable at resolution stitching



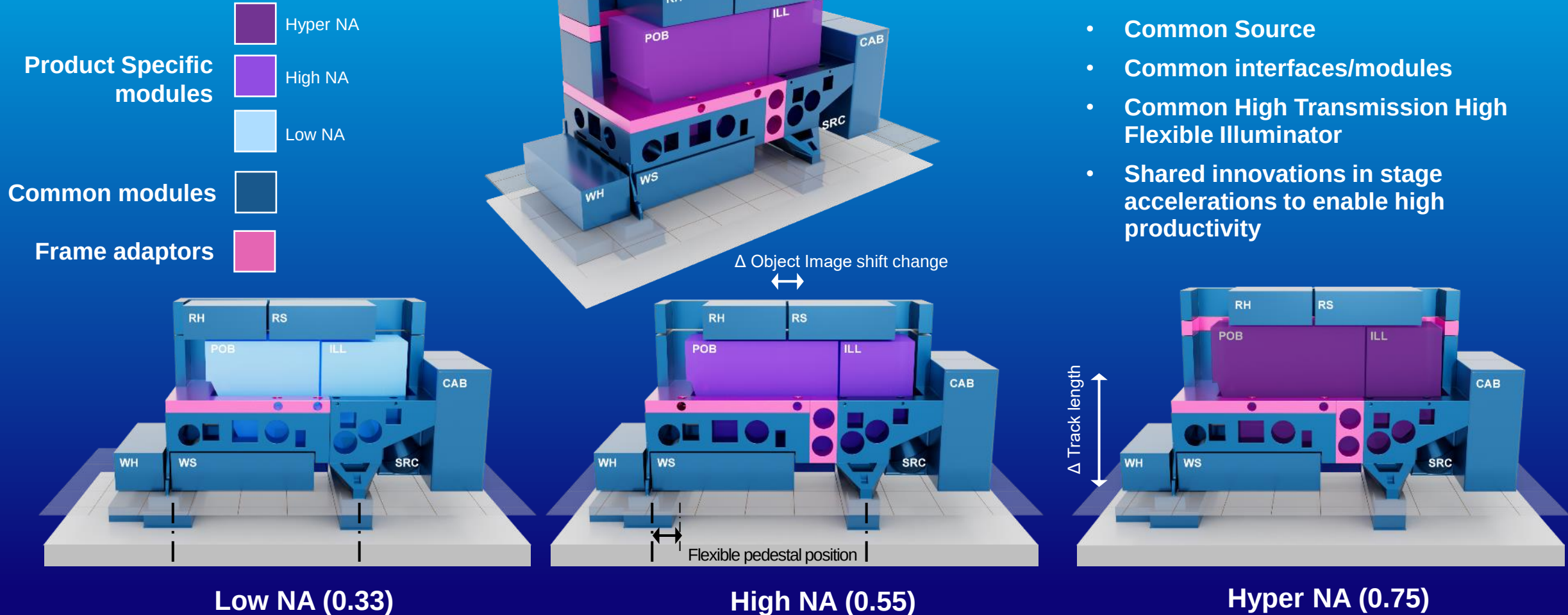
EUV product roadmap enabling affordable scaling

Towards high productivity platform for 0.33NA EUV, 0.55NA EUV and potentially hyper NA in the next decade



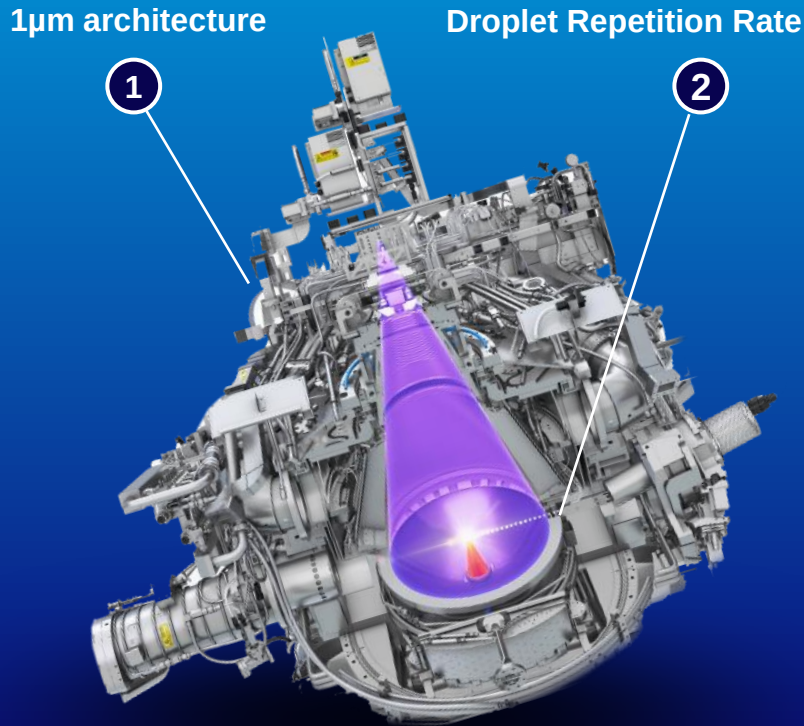
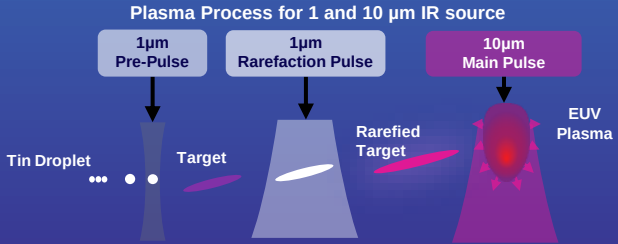
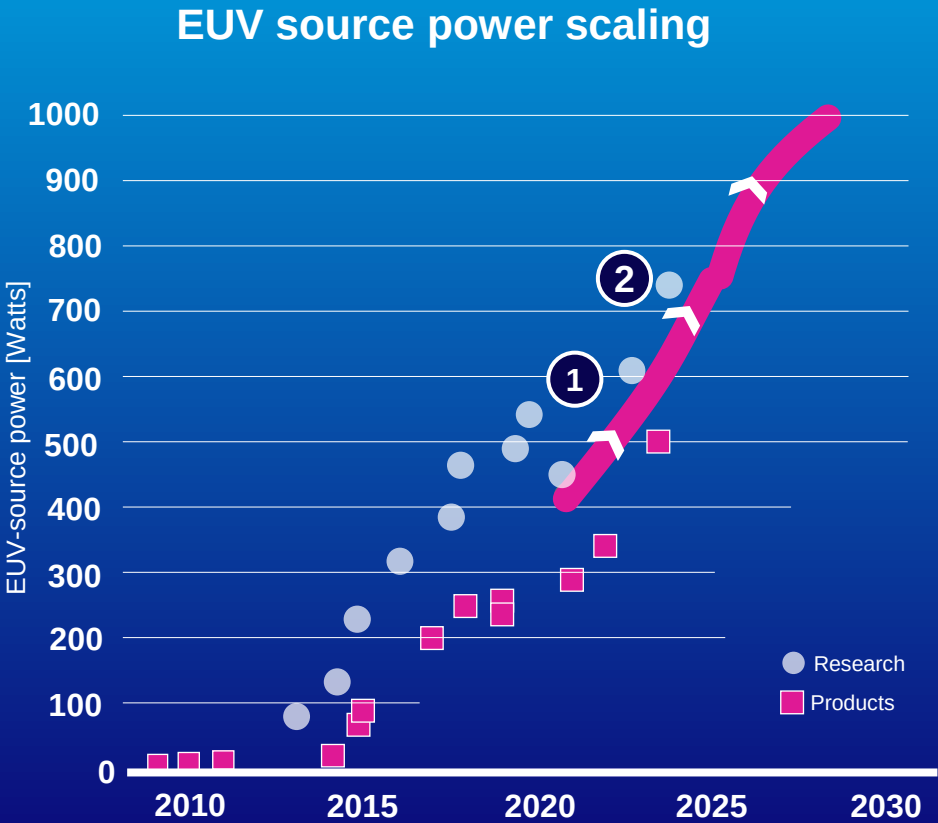
High productivity common platform is enabled by going to one modular frame architecture

Modular Machine Support Frame allows for product mix flexibility in fabs



EUV source power continues to scale with opportunity to achieve >1000W

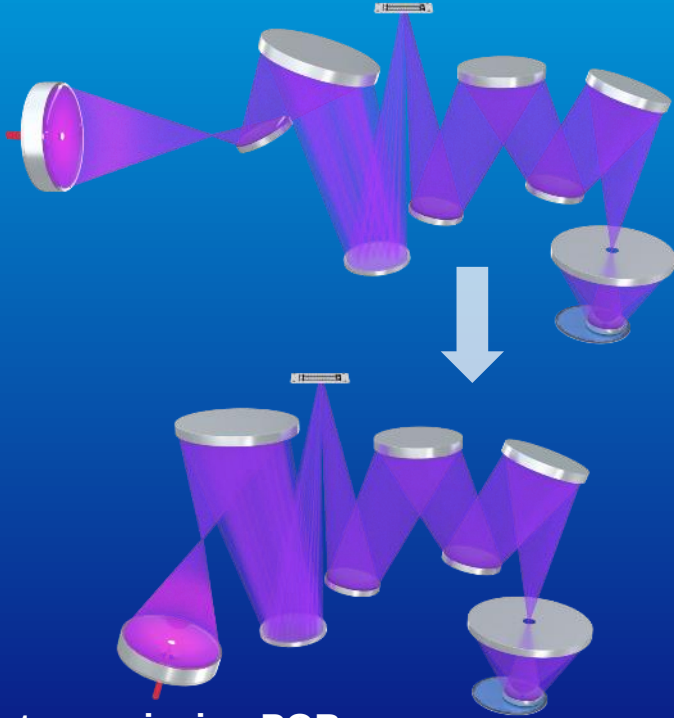
740W EUV power demonstrated - measures identified to reach >1000W in the future



High transmission optics for 0.33 NA and 0.55 NA enable a significant step in productivity

High transmission optics are enabled on the high productivity common platform

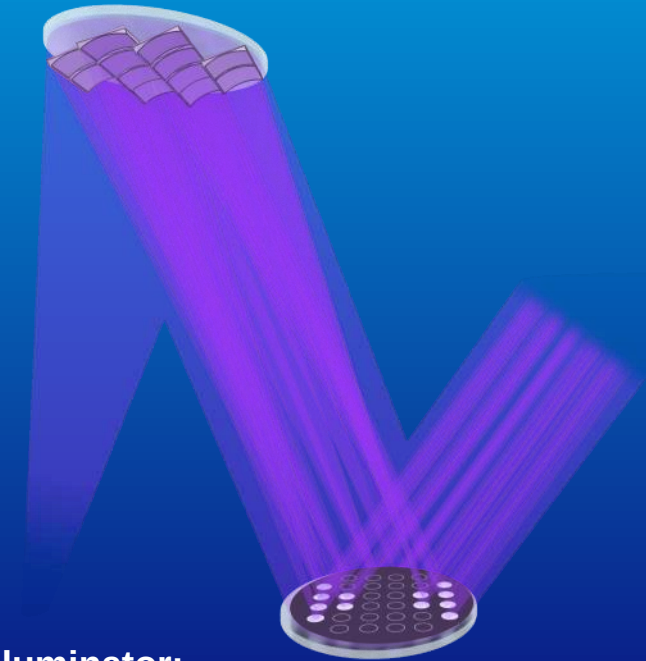
High Transmission POB on 0.33NA



0.33 NA high transmission POB:

- Enable >2x increase in transmission
- Enable scaling of productivity >450 WpH
- Enable common vertical source angle

Flexible illuminator on 0.55NA

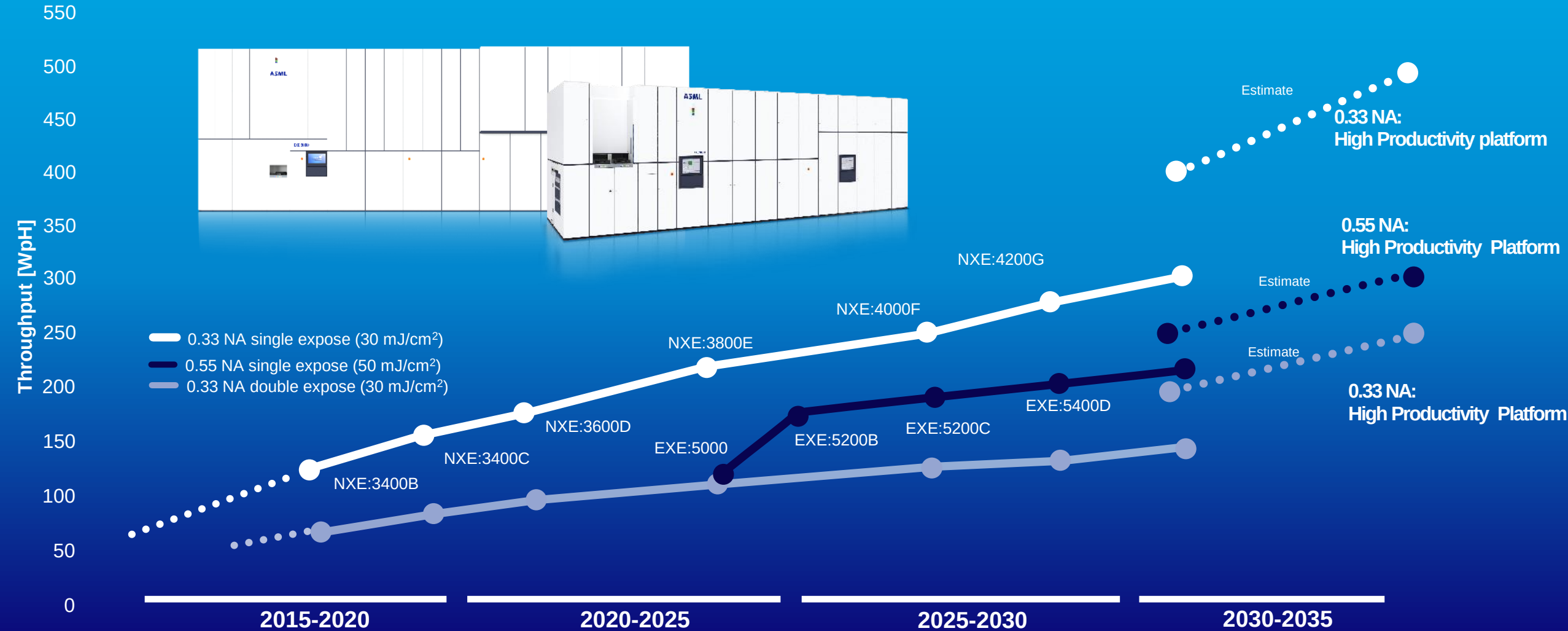


0.55 NA Flexible illuminator:

- Enable ~1.4x increase in transmission
- Productivity scaling of productivity towards 300 WpH
- Enable improved contrast and extension of resolution limits
- Enable common vertical source angle

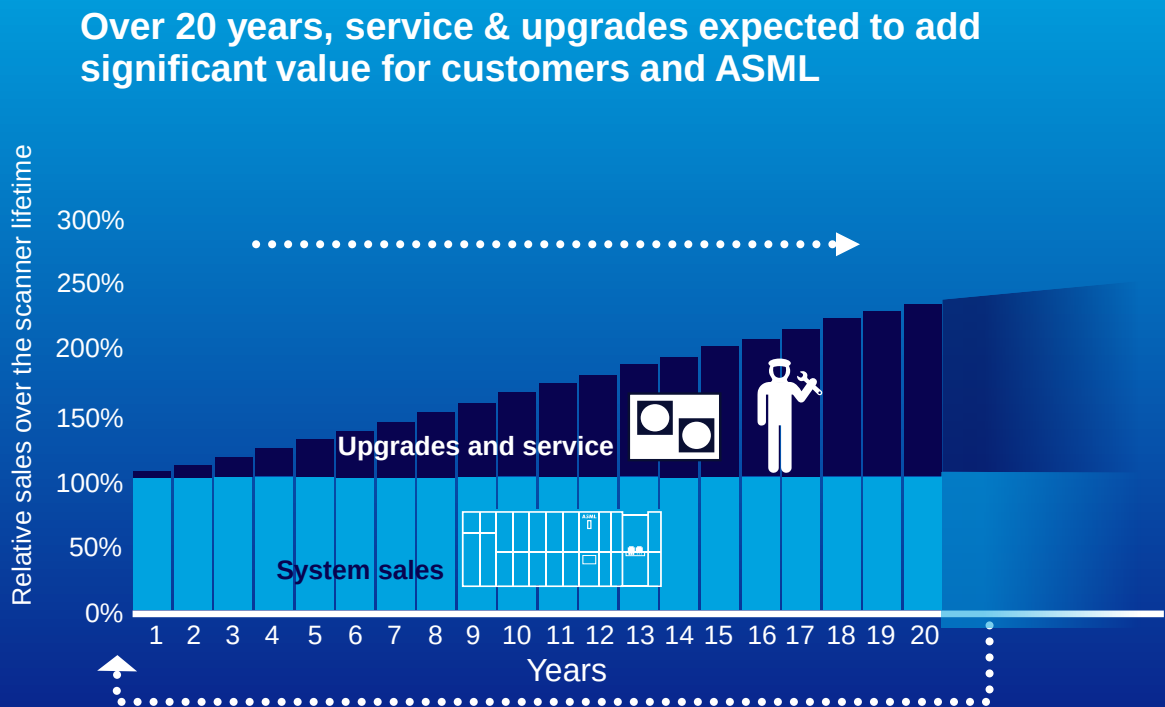
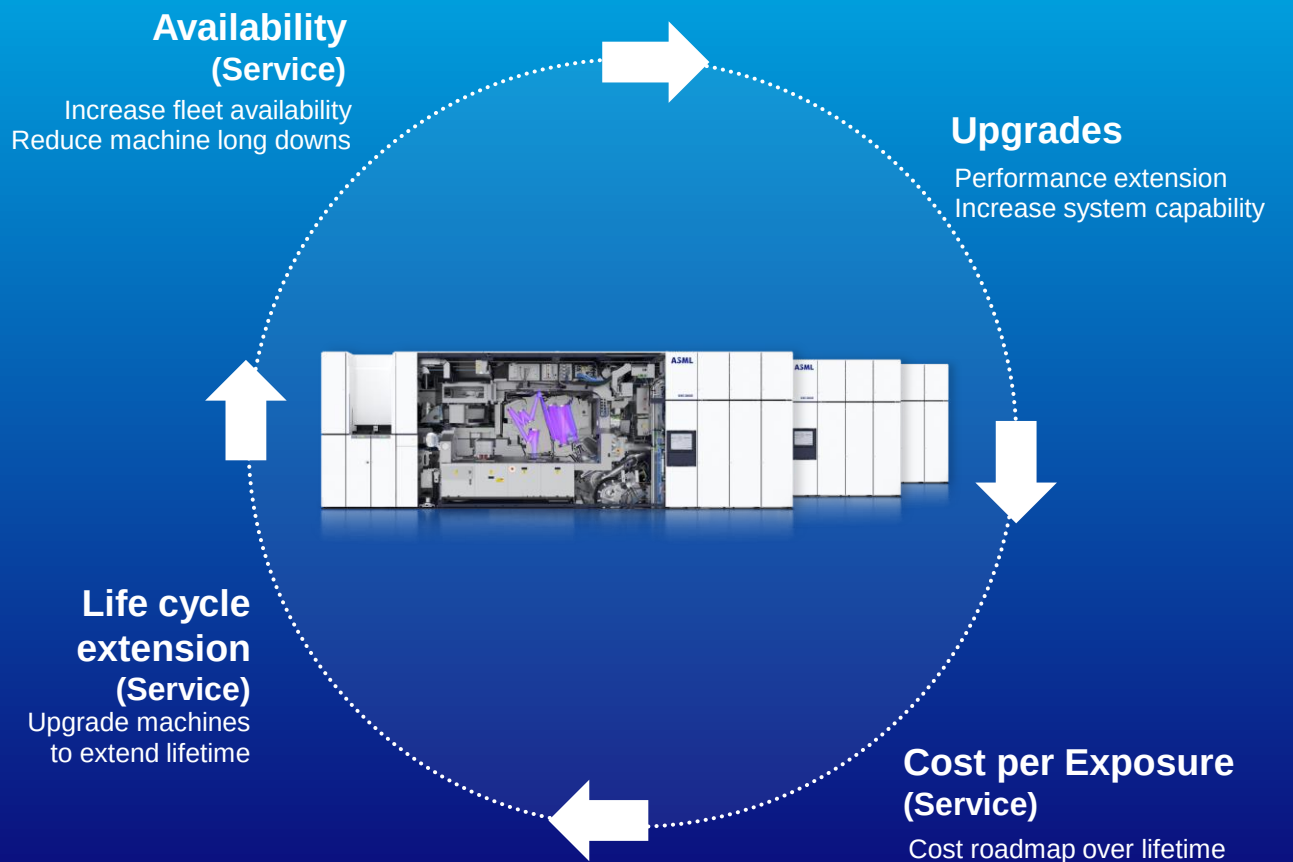
Innovation in optics, source and stages enables scaling of EUV productivity

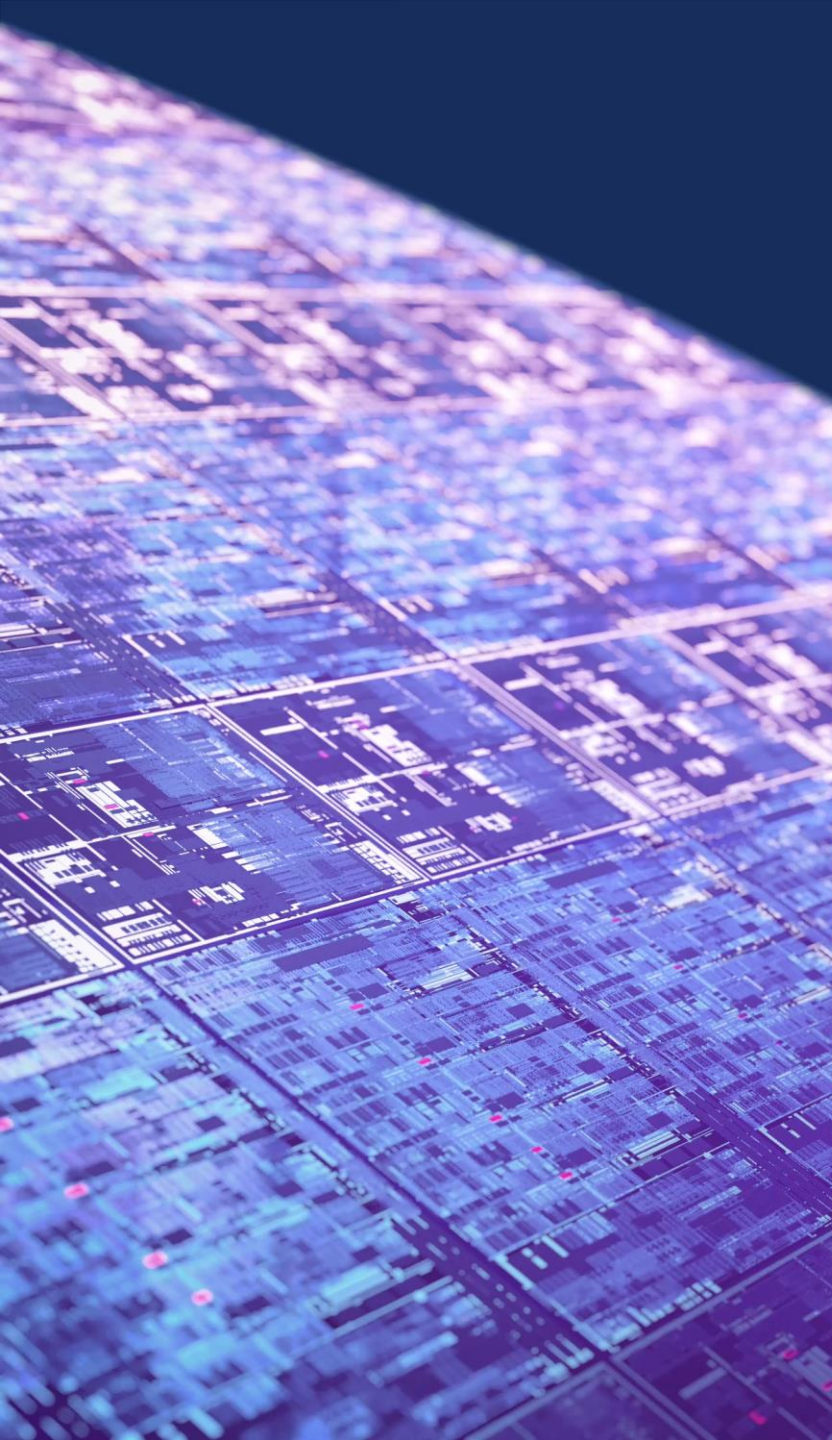
Single patterning 0.55 NA EUV will outperform double patterning 0.33 NA EUV in productivity



EUV Installed Base will further grow in coming years, >20 years lifetime anticipated

ASML supports customers to optimize output of their 0.33 NA EUV & 0.55 NA EUV installed base over lifetime





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Forward Looking Statements

This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DRAM memory, statements with respect to Moore's law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for Applications products, expectations and benefits of a growing installed base, ASML's and its supplier's capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "opportunity", "scenario", "guidance," "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Moore's law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact ASML's business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law.

This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to "greenhouse gas neutral" means remaining emissions, after ASML's efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards.

An aerial photograph of a city grid, viewed from a high angle, with a strong purple and blue color overlay. The grid lines are clearly visible, and the overall image has a futuristic, digital feel. The text "THANK YOU" is overlaid on the right side of the image in a white, sans-serif font.

**THANK
YOU**