



Small Talk 2024

Holistic Lithography Solutions and business opportunity

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Executive Vice President and Head of Business Line Applications

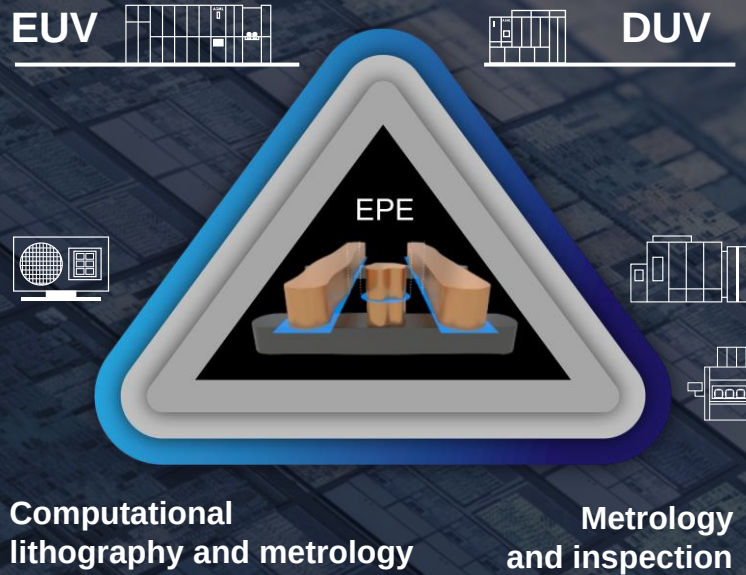
ASML Investor Day

Veldhoven, The Netherlands
November 14, 2024

Holistic Lithography Opportunity & Growth Drivers

- **Holistic Lithography** focuses on improving **Accuracy** and **Patterning Yield** for our customers.
- **Accuracy:** drive improvements in Overlay and Edge Placement Error (EPE) via Computational Lithography (physical models & AI), Metrology & Inspection and Scanner Optimization.
- **Patterning Yield:** drive cost effective **metrology and inspection** solutions for both **2D and 3D** structures enabling early yield ramp and holistic lithography control
 - Significant progress on multi e-beam inspection and the opportunity for HVM, first application will be Voltage Contrast inspection
 - Followed by smaller 2D features and 3D structures requiring buried defect inspection
- **Enable** front end 3D integration (**wafer bonding**) with **metrology and control solutions** to meet customer **overlay** requirements.
- The Holistic Lithography business is expected to grow at >15% CAGR with strong gross margins from 2025 to 2030.

Lithography scanner
with advanced control capability



Holistic lithography enables our customers to maximize Good Wafers per Day

Our product portfolio focuses on Patterning Yield and Accuracy





Patterning Yield

- Patterning process control
- Optical metrology
- E-beam metrology
- E-beam inspection
- AI based models



$$CD = k_1 \frac{\lambda}{NA}$$

Resolution

- Advanced ArFi
- EUV 0.33 NA
- EUV 0.55 NA





Accuracy

- Overlay
- Local CDU
- Edge Placement Error (EPE)





Productivity

- System Throughput
- Overall equipment efficiency



System cost

/



Lifetime

+



Operational cost

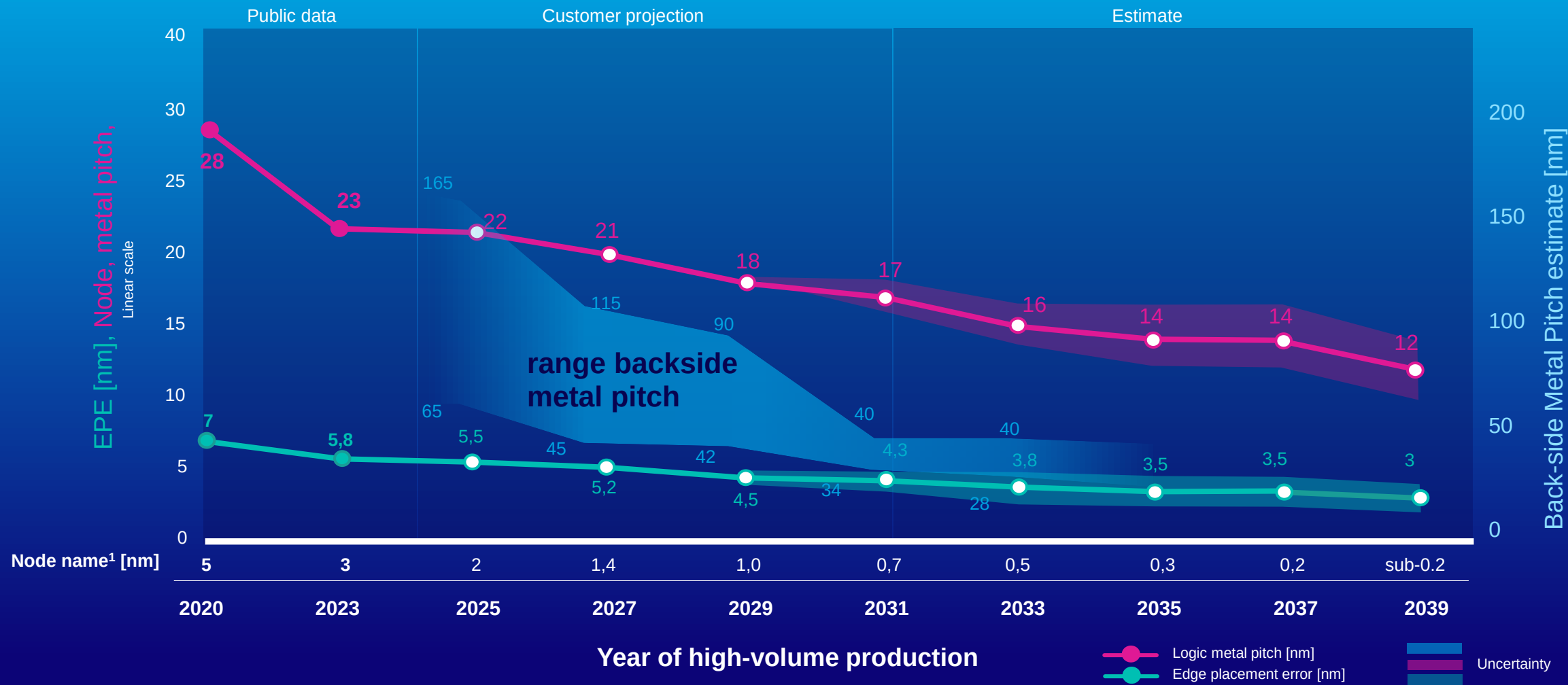
+



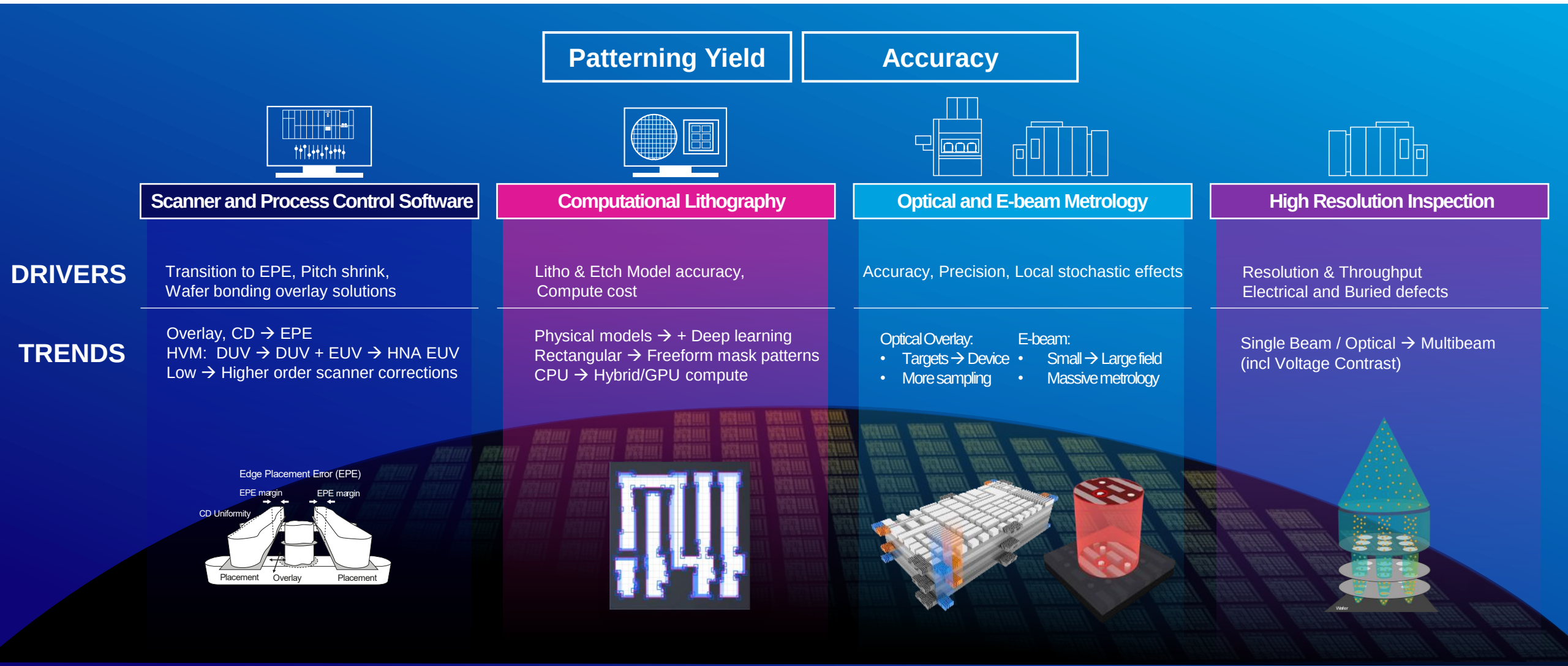
Environmental cost

1 Ton CO₂ = 200 EUR

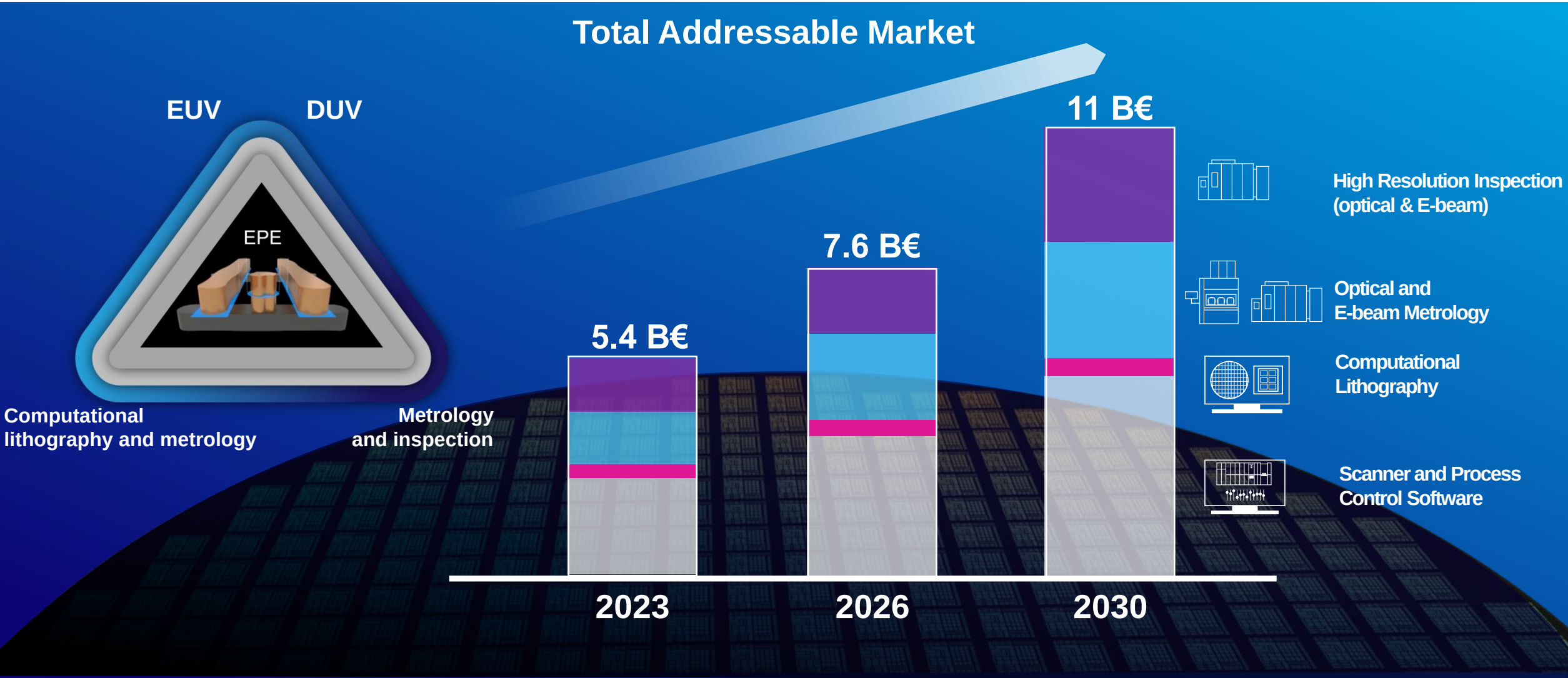
Logic roadmap continues to drive shrink, requires improvements in Edge Placement Errors, tightens backside metal pitch and post bonding overlay



Evolving Industry Roadmap drives growth opportunity for Applications Products

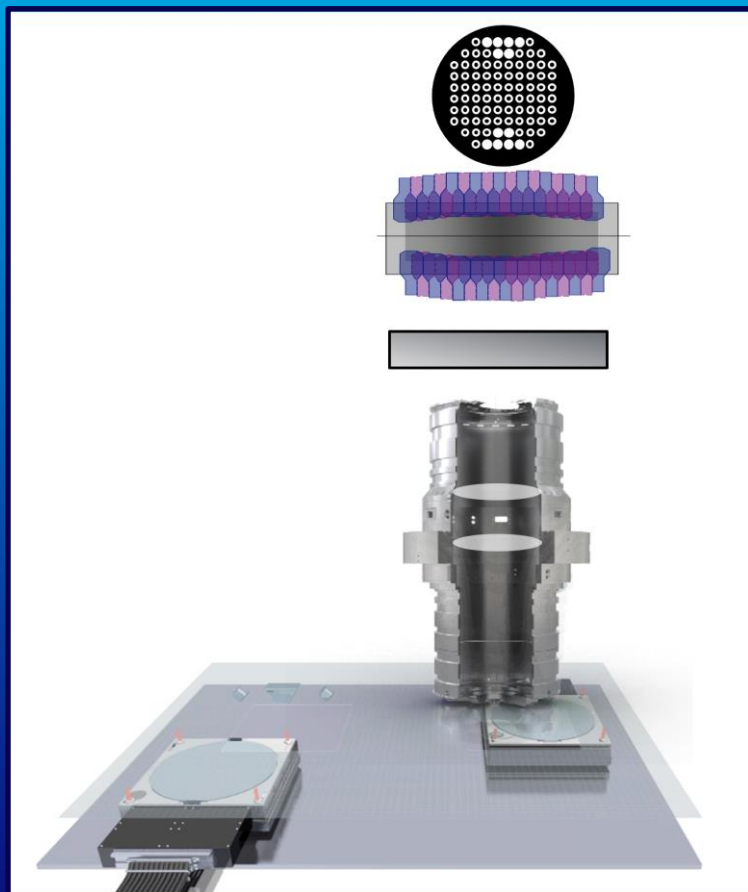


Evolving Industry Roadmap drives growth opportunity for Applications Products



Lithography is a formidable tool to compensate process fingerprints

Correction capability increased ~5 orders of magnitude

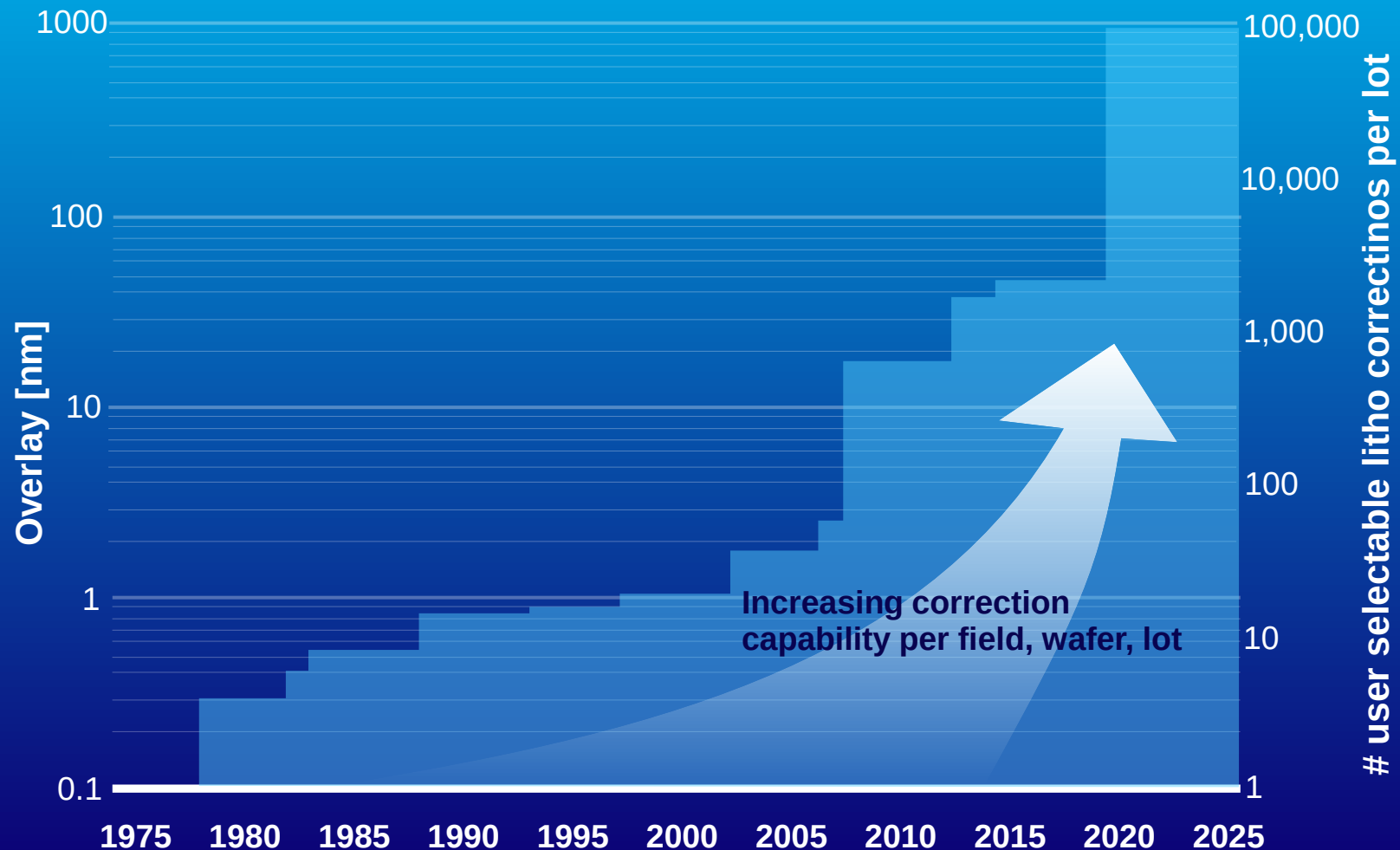


Metrology stage

100% of wafers
are measured

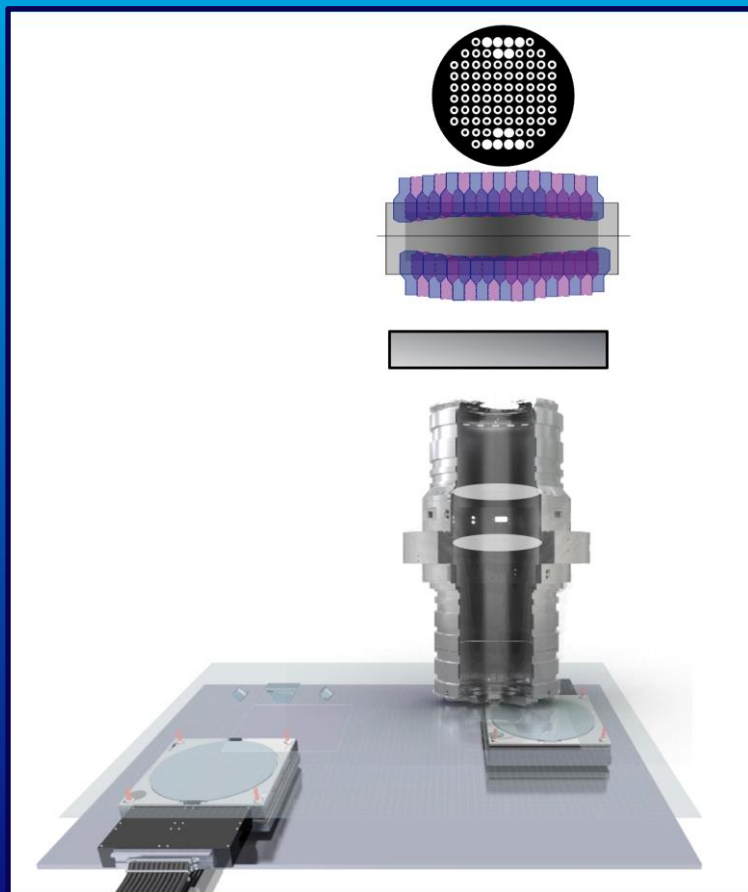
Exposure stage

100% of wafers are
processed field-by-field



Holistic approach improved overlay ~3 orders of magnitude

Correction capability increased ~5 orders of magnitude and overlay improved ~3 orders of magnitude

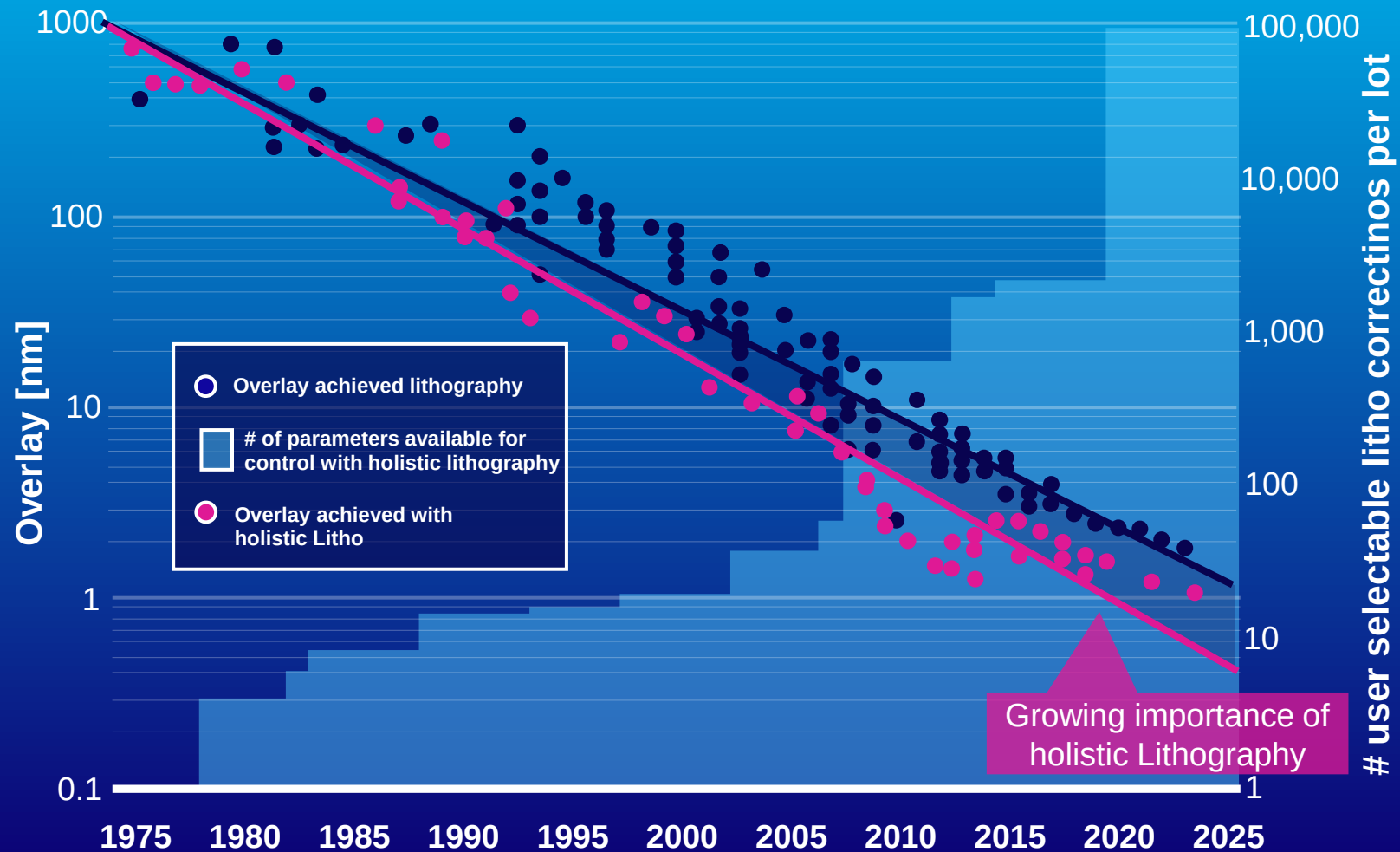


Metrology stage

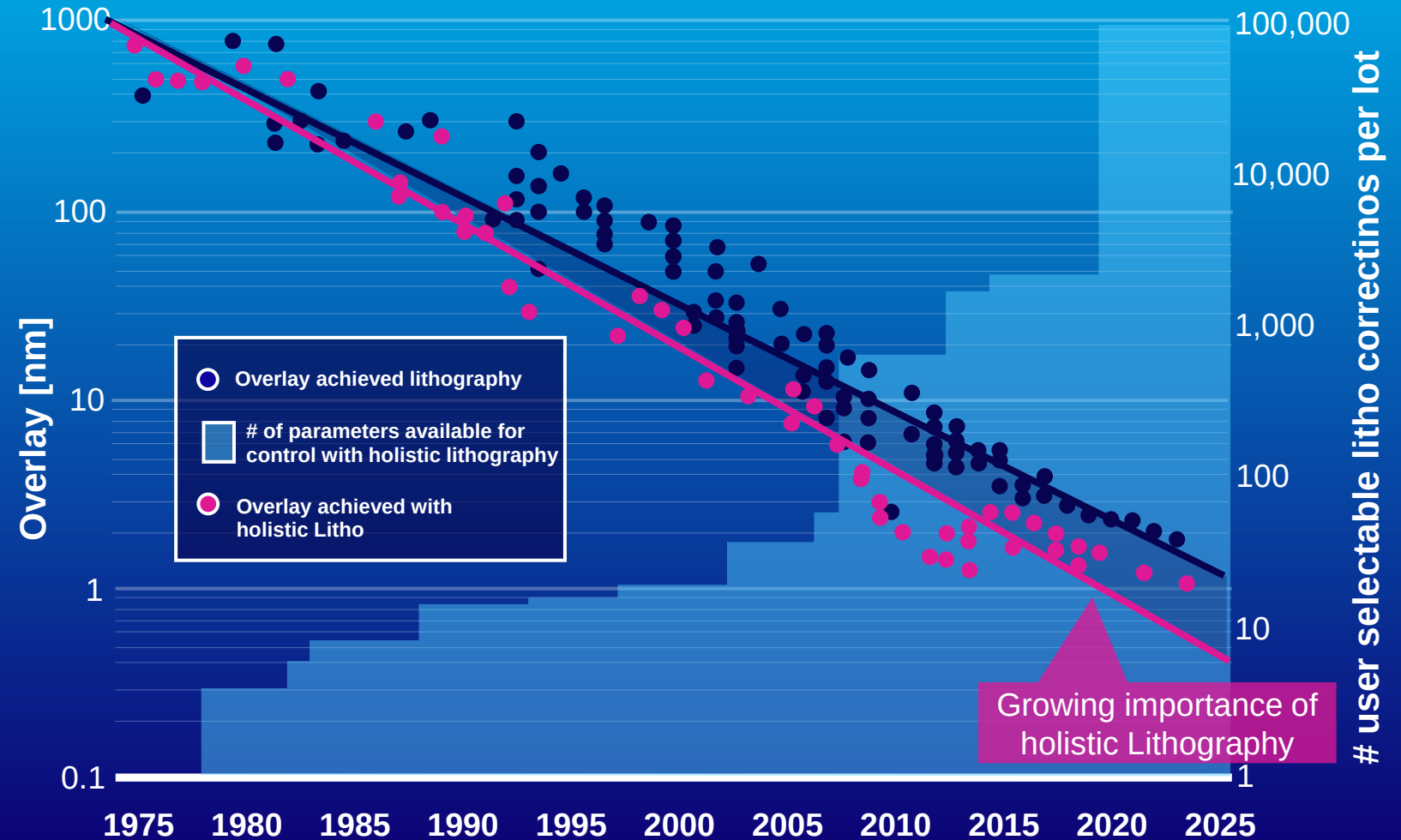
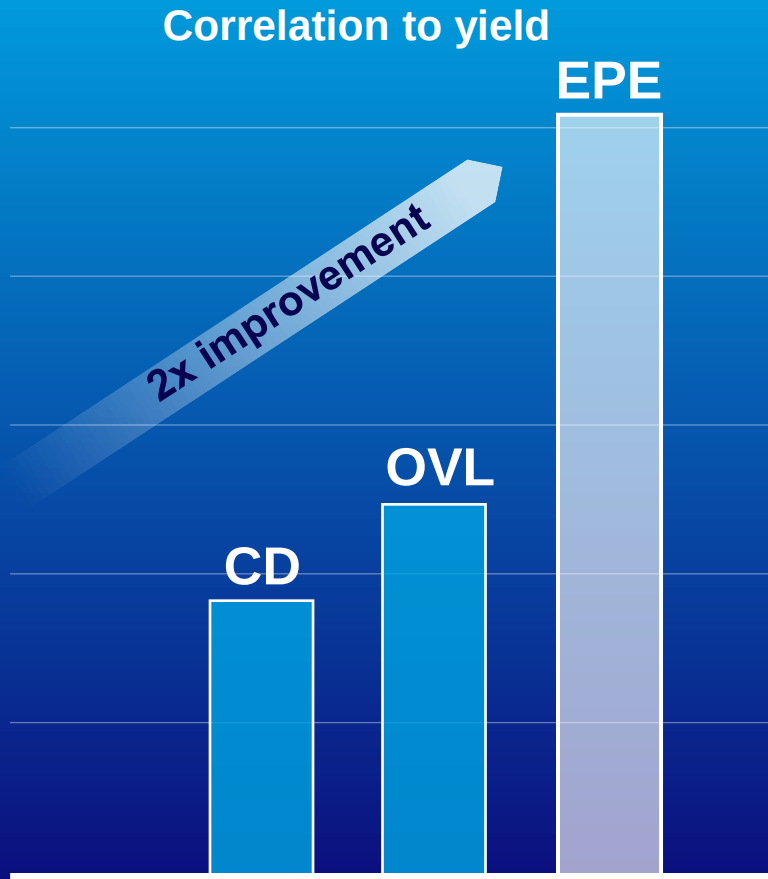
100% of wafers
are measured

Exposure stage

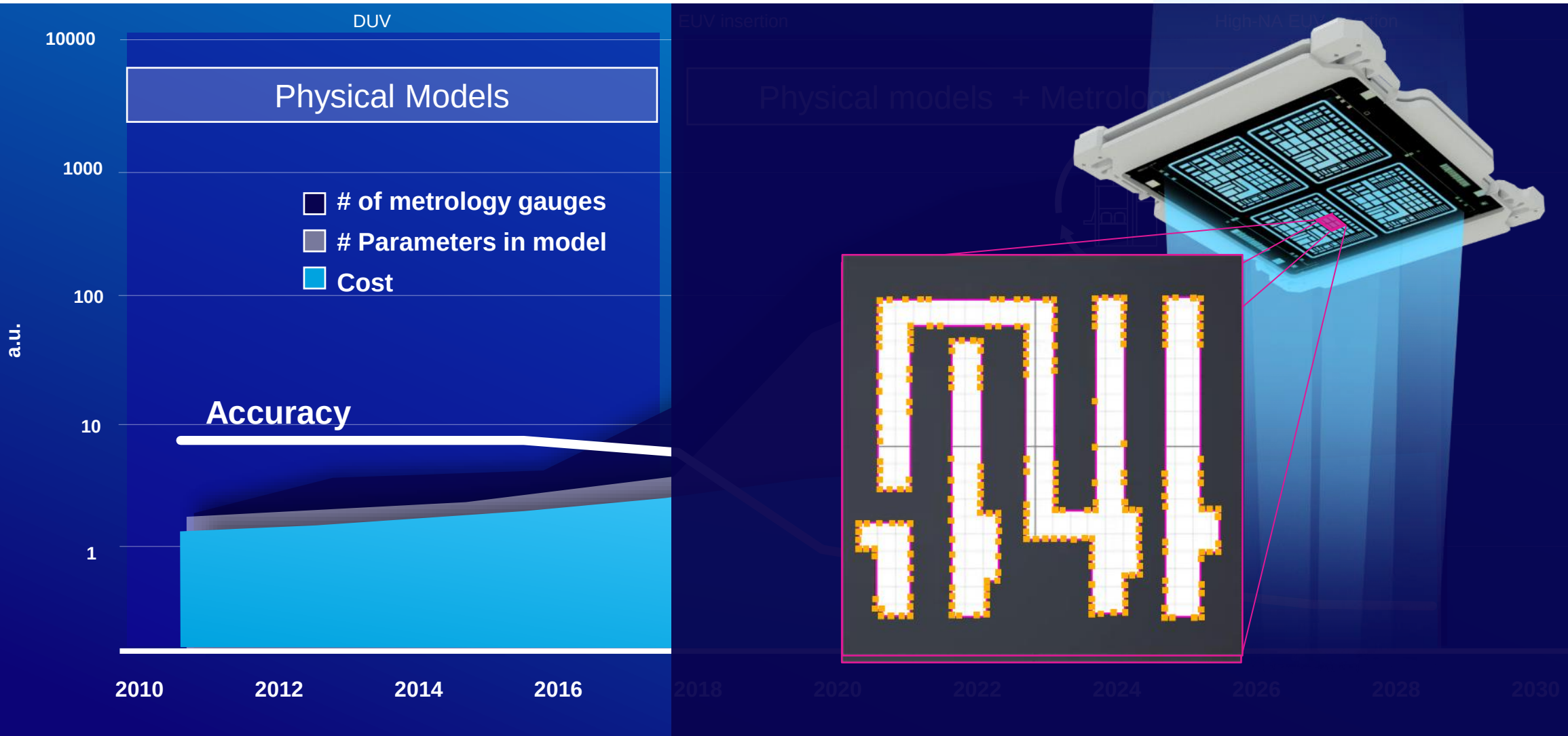
100% of wafers are
processed field-by-field



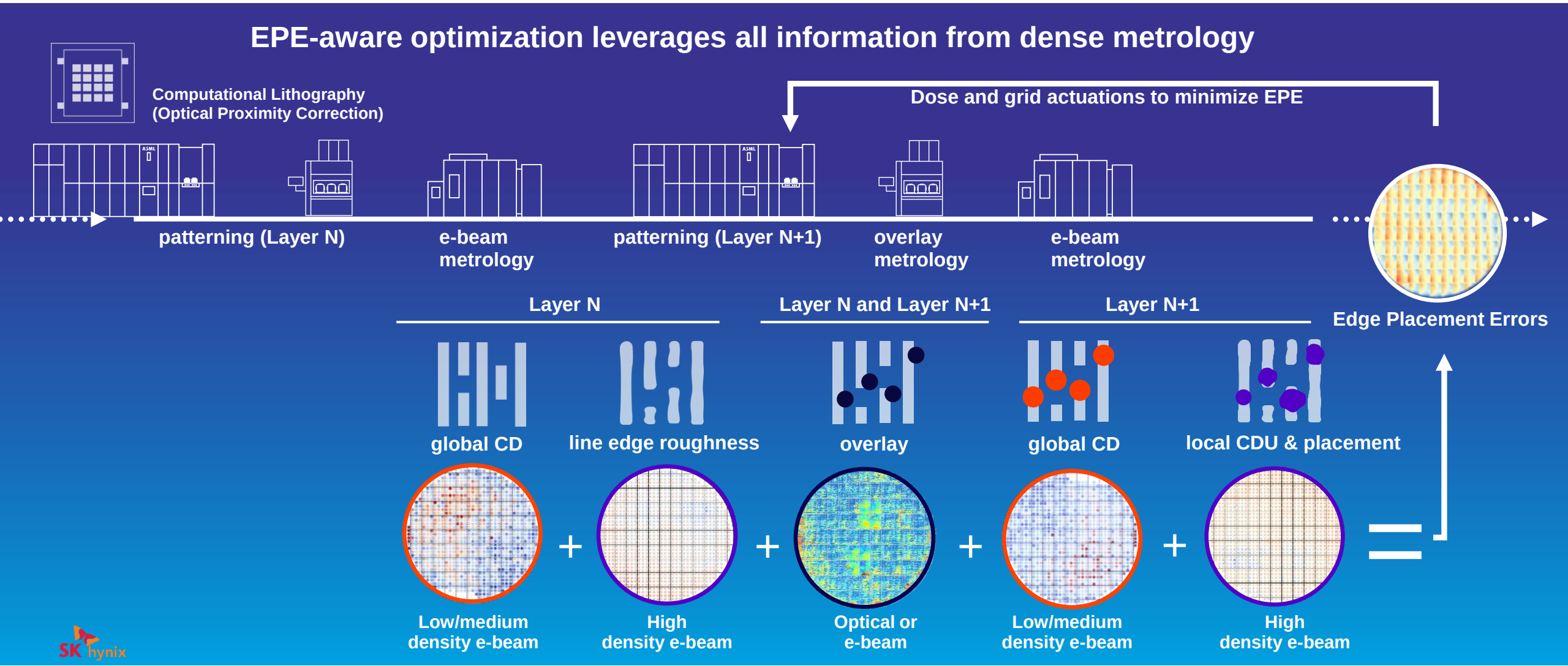
Holistic approach improved overlay ~3 orders of magnitude and extending to EPE gives another opportunity to improve Yield



Computational litho: optical proximity correction accuracy has improved rapidly thanks to the introduction of machine learning and massive metrology

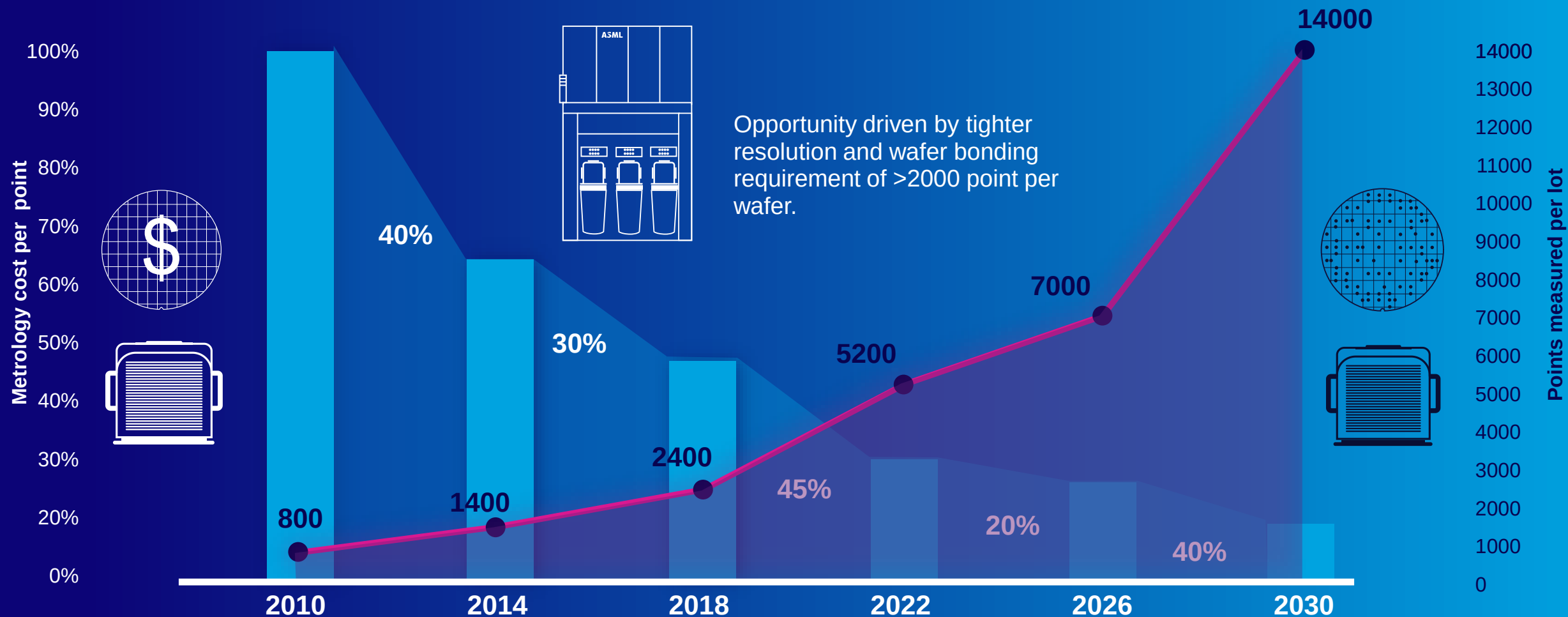


Optimizing Patterning Yield by combining metrology data and translating this to scanner actuations

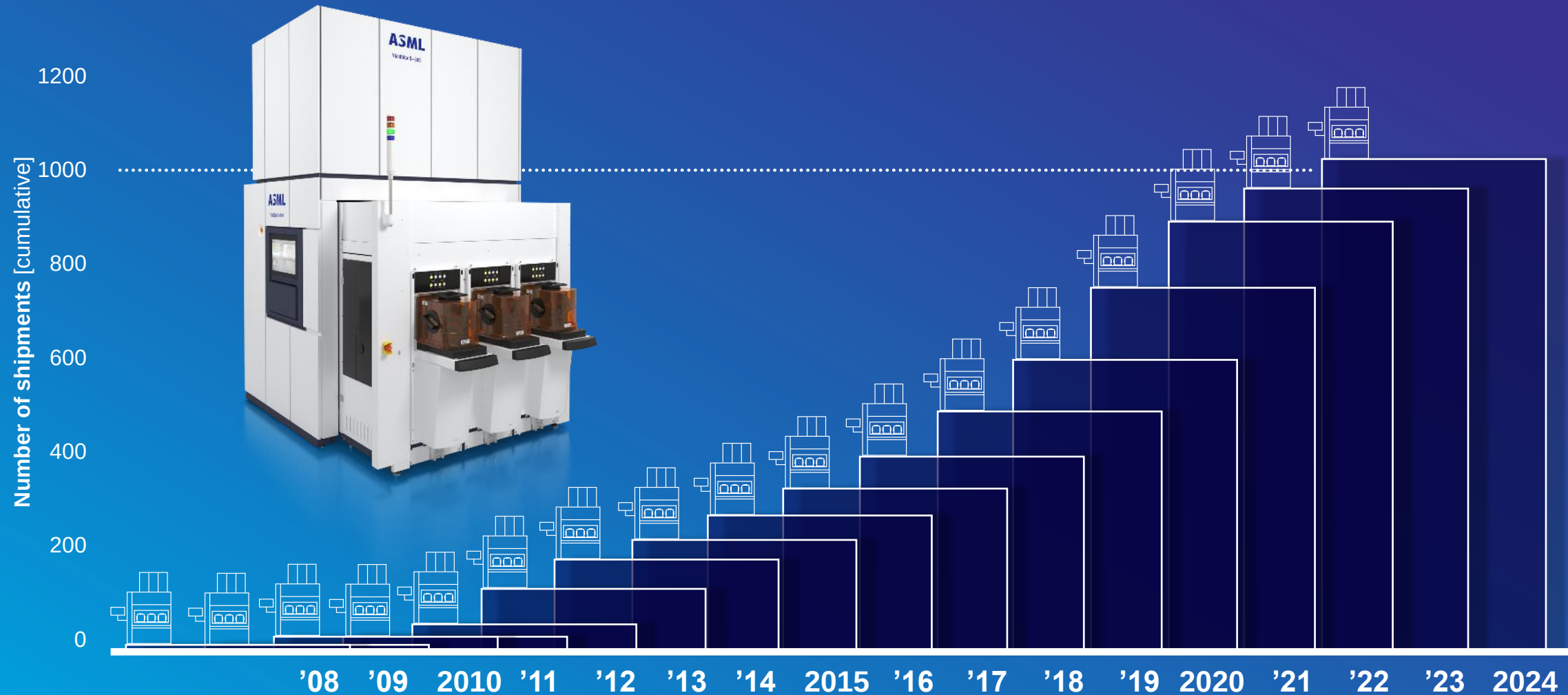


Massive overlay metrology is needed to drive those scanner corrections

YieldStar platform enables increase of sampling by 80% while cost effectiveness is improved by 30~45% every 4 years

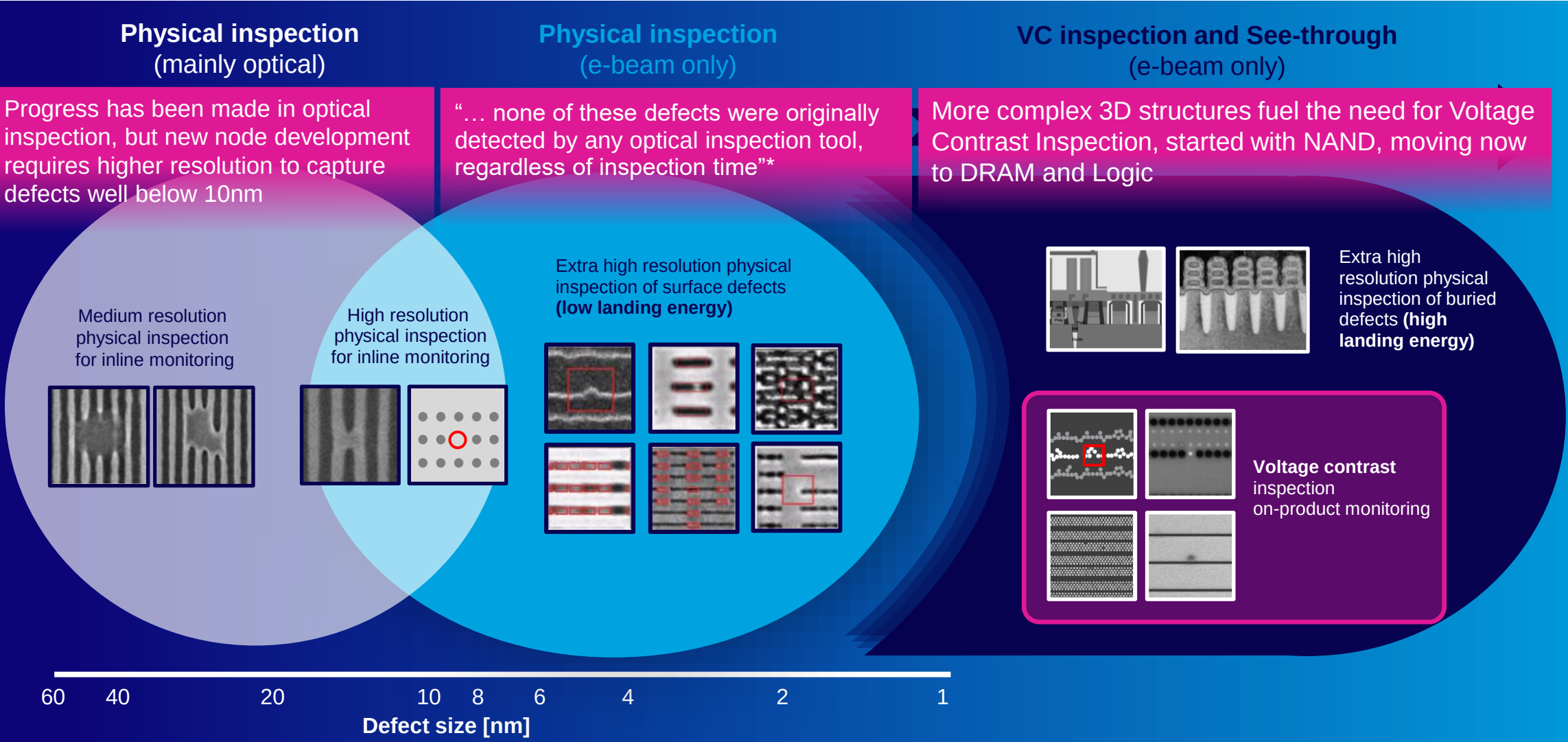


YieldStar installed base reached >1000 systems in H1'24



Patterning Yield: e-beam opportunity for physical, buried defects and voltage contrast

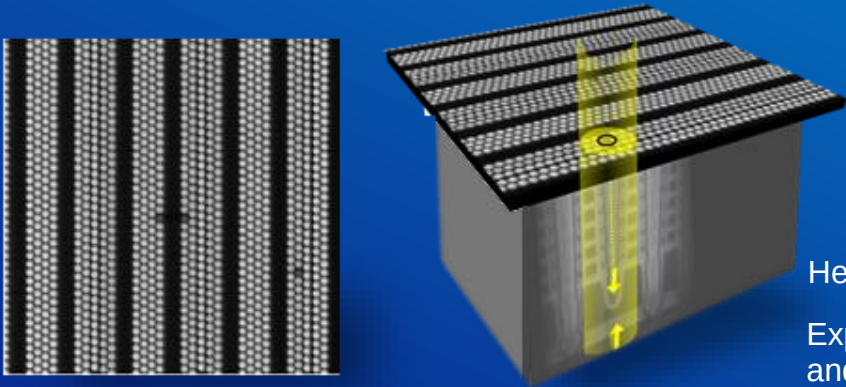
Voltage contrast is driving the insertion of e-beam inspection in High Volume Manufacturing



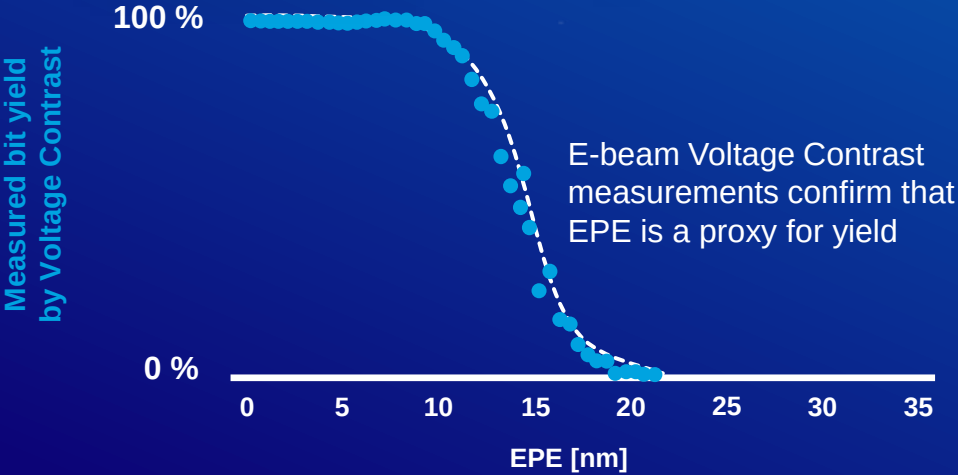
Voltage contrast inspection adopted in NAND HVM, expanding to Logic and DRAM

Unique capability of electron beam inspection to find yield limiting defects

VC inspection: detection of interlayer defects causing electric opens and shorts



Heavily used in 3D NAND
Expanding usage in DRAM and Logic

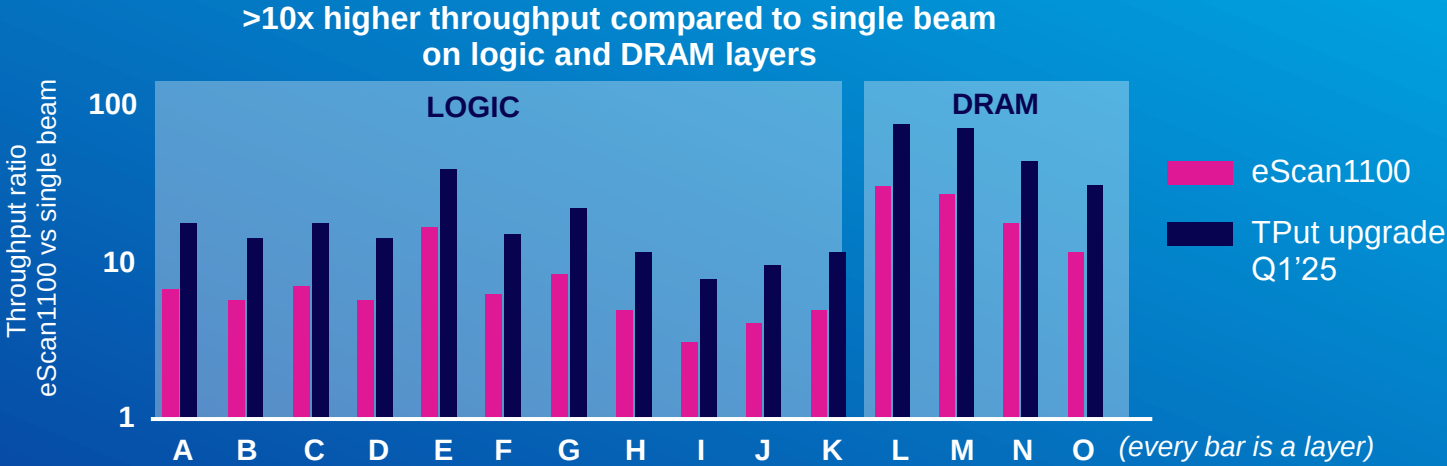


Voltage Contrast Inspection
Installed Systems (2019-2023)

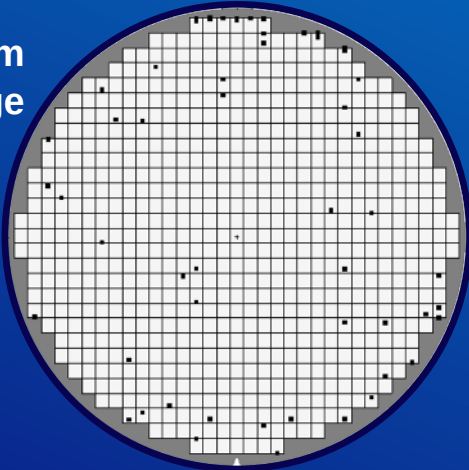


Multibeam eScan 1100, larger wafer coverage and better CoO, enabled by >10x throughput

>10 eScan1100 systems at >5 customers for evaluation and qualification for Voltage Contrast in HVM

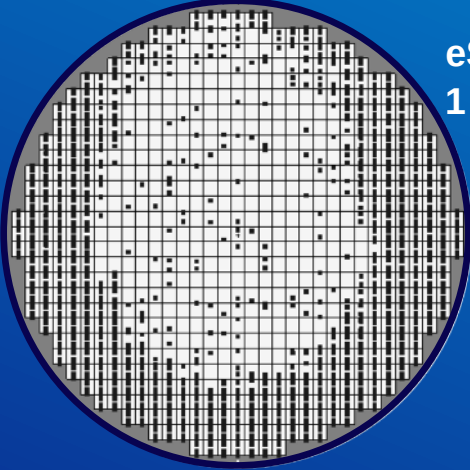


single beam
0.1 - 0.2% coverage



Limited die sampling unable to catch wafer defect signature

eScan1100 (multi beam)
1 - 2% coverage

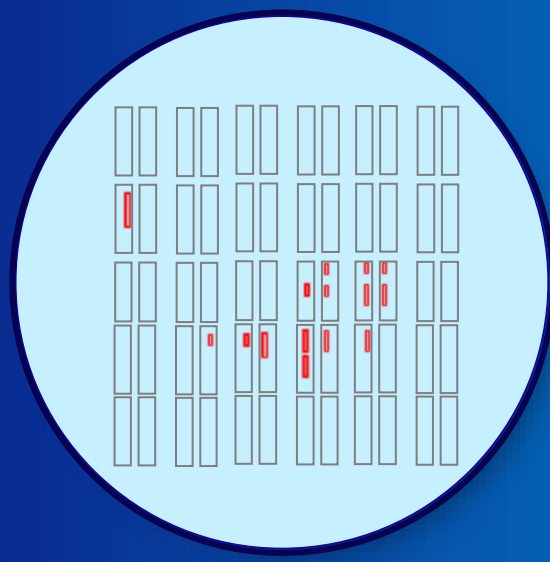
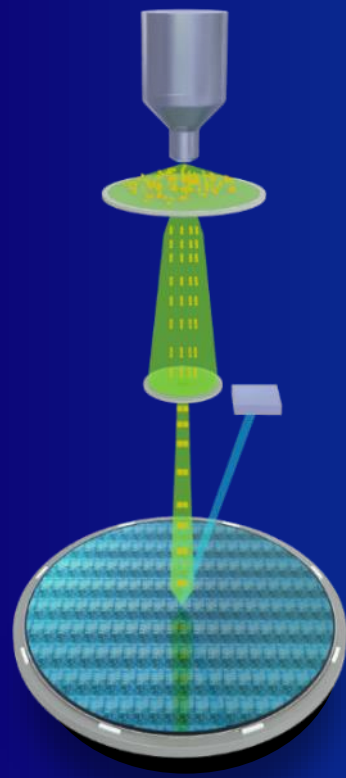


100% die sampling captures clear wafer defect fingerprint

- Demonstrated value in customer evaluations: larger wafer coverage capable of capturing **wafer defect fingerprints** for **inline monitoring**, enabled by faster throughput and lower cost of ownership

Customer data shows eScan1100 capturing clear defect signature with higher throughput

7~8x larger wafer coverage and ~60% shorter cycle time

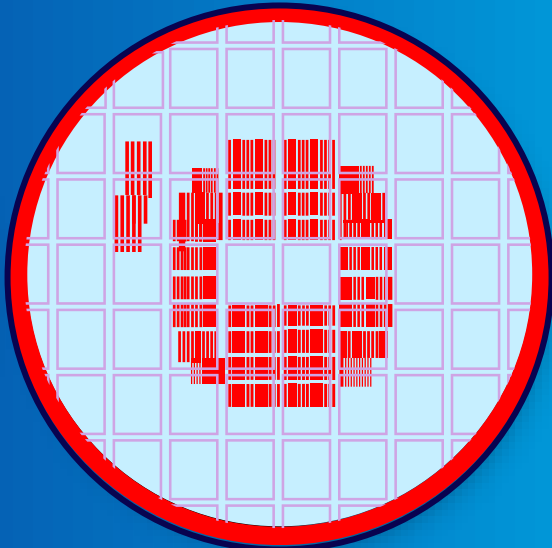


Single Beam Inspection

Wafer coverage: 0.2%

Inspection time: 100%

Miss the signature



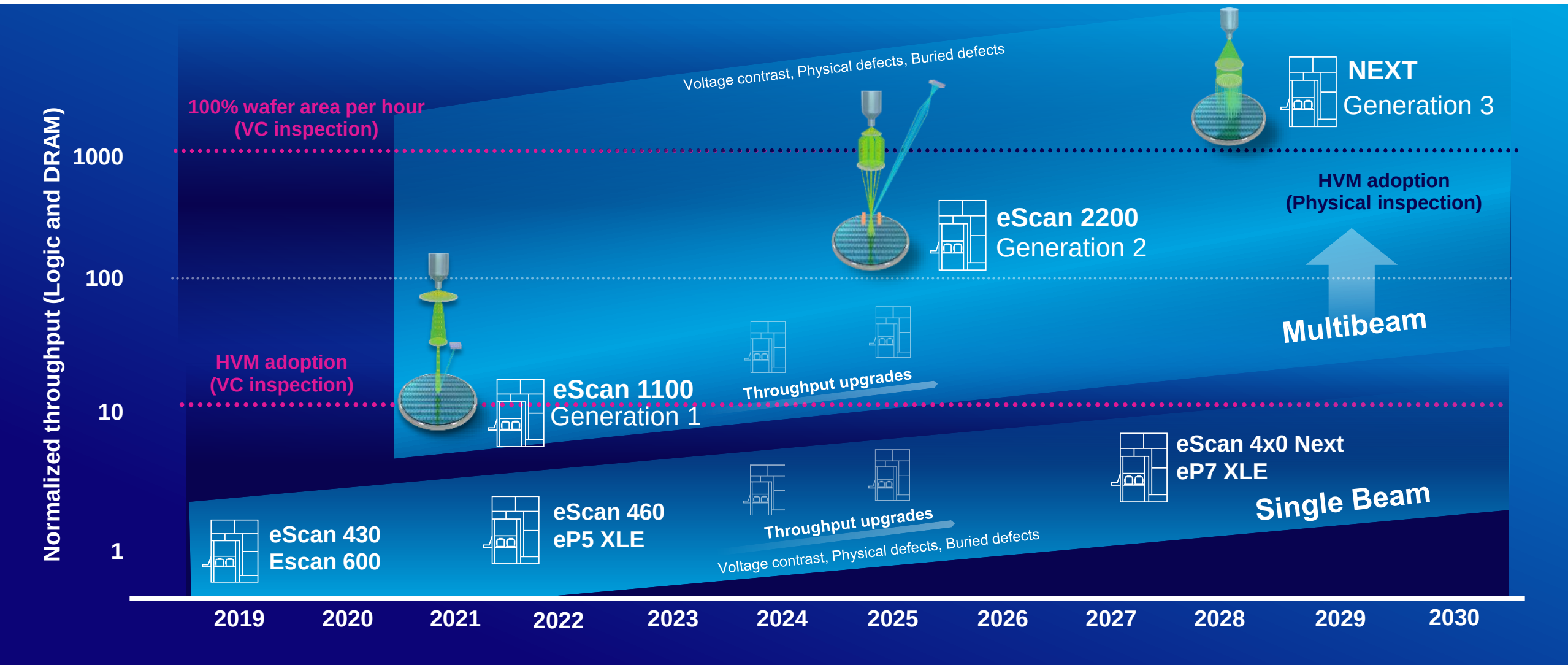
eScan1100

Wafer coverage: 1.5%*

Inspection time: ~40%

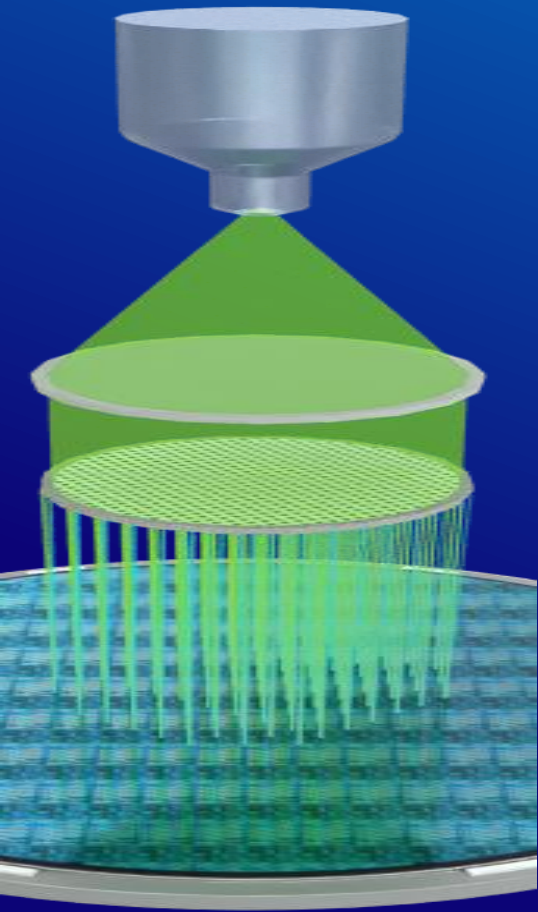
Clear defect signature

Multibeam enables higher throughput and larger wafer coverage in voltage contrast and physical inspection for inline defect monitoring in HVM



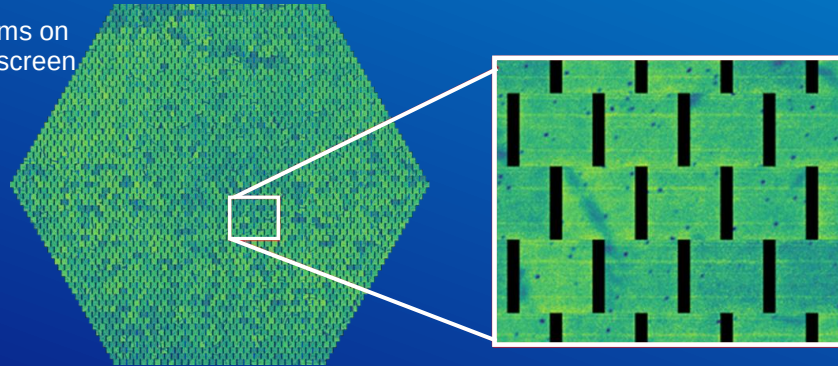
Next step in multibeam: from 25 to >2700 beams

Technology demonstration ongoing, working towards customer early access in 2025



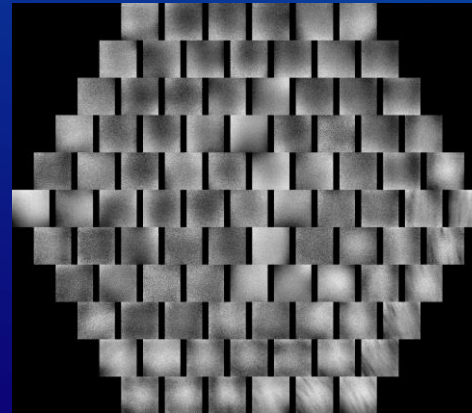
Focal plane verification

>2700 beams on
scintillator screen

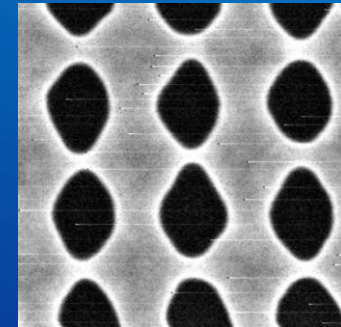


Through focus measurement

All of >2700
beams on
scintillator screen
are functional



Detector functionality and resolution verification



Sample image

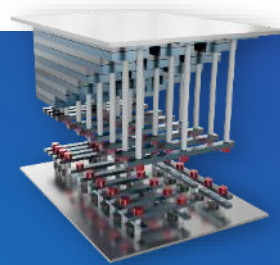
We expect front end 3D integration to complement 2D shrink in driving density

Front end 3D integration challenges will trigger new litho opportunities for all semiconductor products

NAND

DRAM

LOGIC



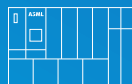
3D NAND

HVM >2030



W-W hybrid

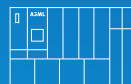
50nm → 25nm



KrF

W-W / D-W hybrid

50nm → 25nm



KrF



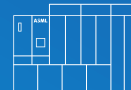
4F² 2D ARRAY

>2027 >2032



W-W hybrid

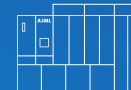
6nm → 3nm



ArFi

W-W / D-W hybrid

6nm → 3nm



ArFi



3D ARRAY

>2032

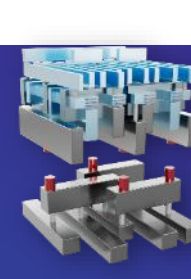


W-W hybrid

>4.5nm



ArFi



BSPN

2026



W-W Fusion

2.5nm → 1.6nm



NXE/EXE



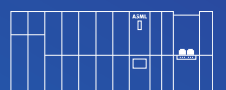
CFET

>2032



W-W | D-W Fusion

5nm → 2nm



NXE/EXE

Stack

Bonding

Overlay

Litho

Holistic Lithography will enable 3D integration

Metrology and scanner control at pre and post bonding critical process points needed for overlay

Pre-bonding < 5 nm overlay error

Bonding



Both wafers have separate patterning and processes but overlay needs to be matched between them prior to bonding

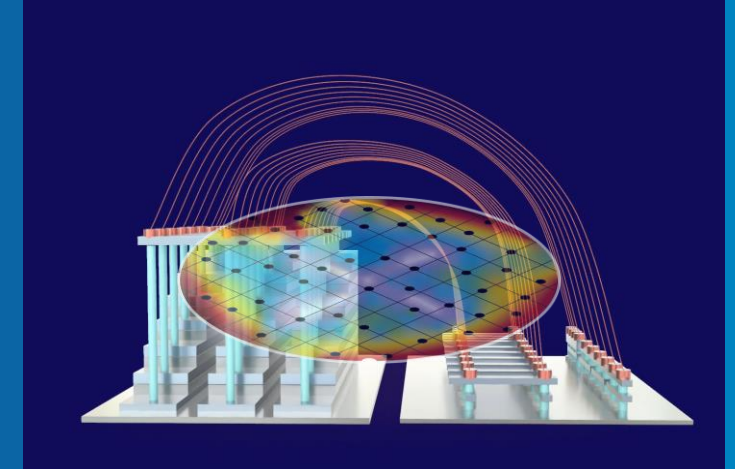
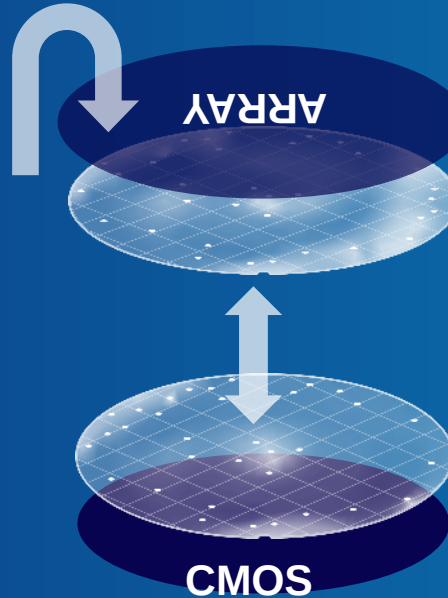
1

Scanner and offline metrology

2

Scanner correction and control

Actuators

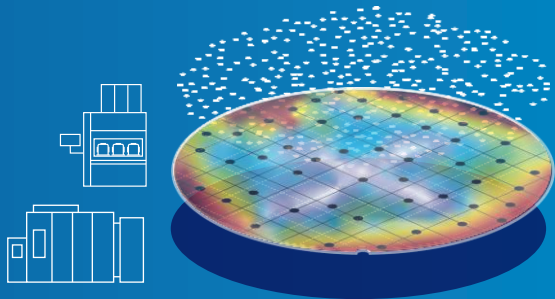


Holistic Lithography will enable 3D integration

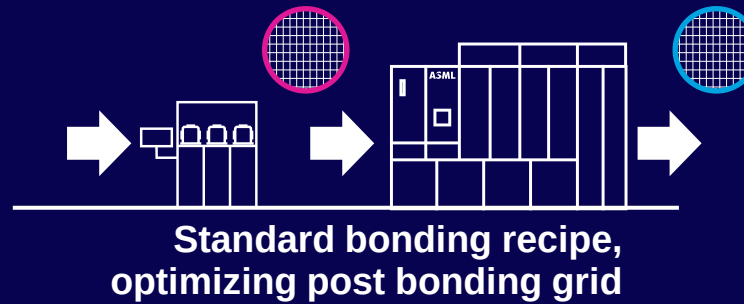
Metrology and scanner control at pre and post bonding critical process points needed for overlay

Bonding >50nm overlay error
>5000 measurements/wafer

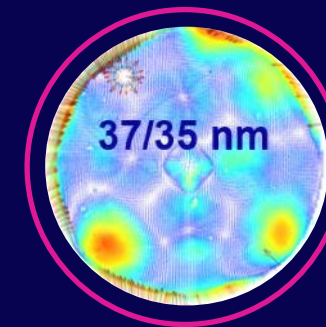
Bonder creates a massive deformation on the wafer



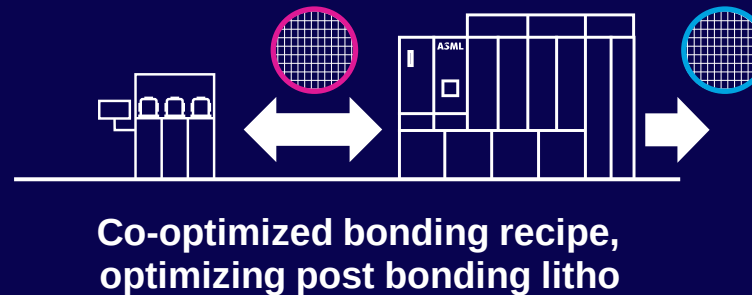
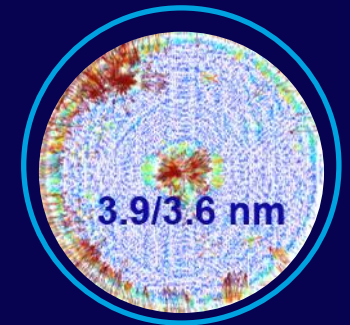
Requires massive metrology on every wafer to categorize the large (local) variety in fingerprint



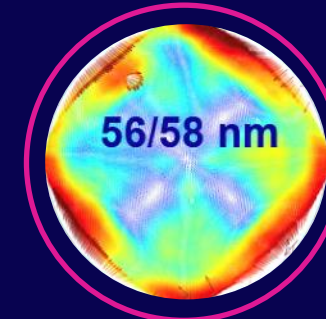
Wafer deformation directly after bonding



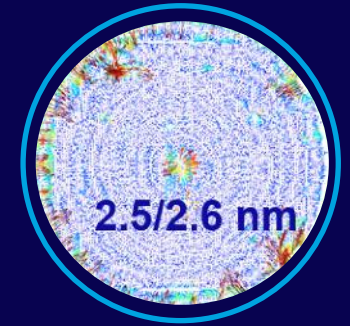
Overlay error after litho correction



Wafer deformation directly after bonding



Overlay error after litho correction

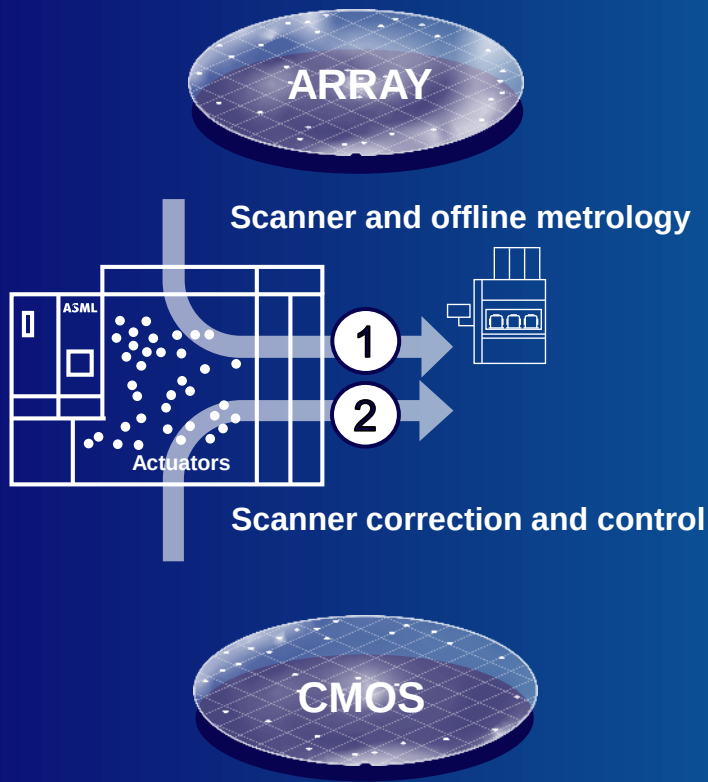


Holistic Lithography will enable 3D integration

Metrology and scanner control at pre and post bonding critical process points needed for overlay

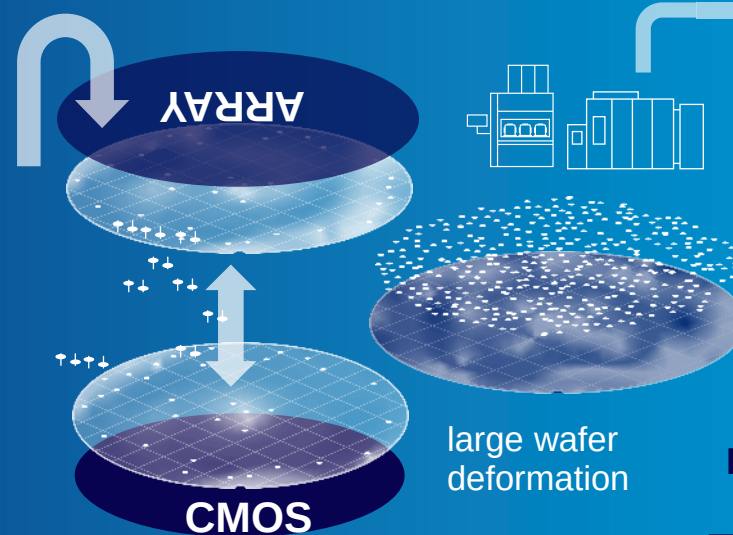
Pre-bonding

< 5 nm overlay error



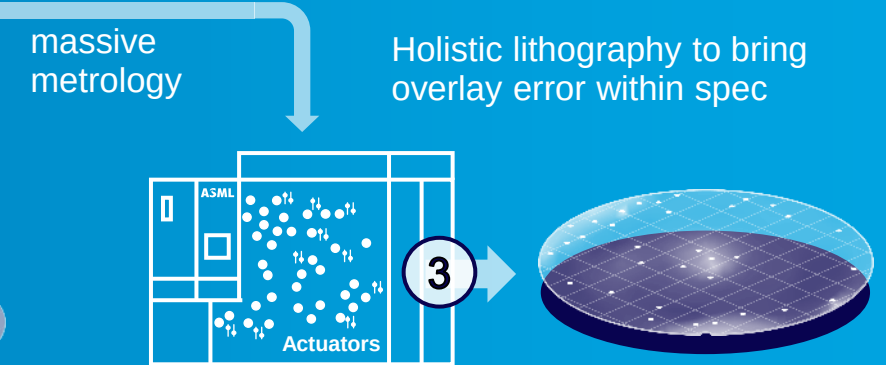
Bonding

50~100nm overlay error
>5000 measurements/wafer



Post-bonding

< 5 nm overlay error
>2000 measurements/wafer



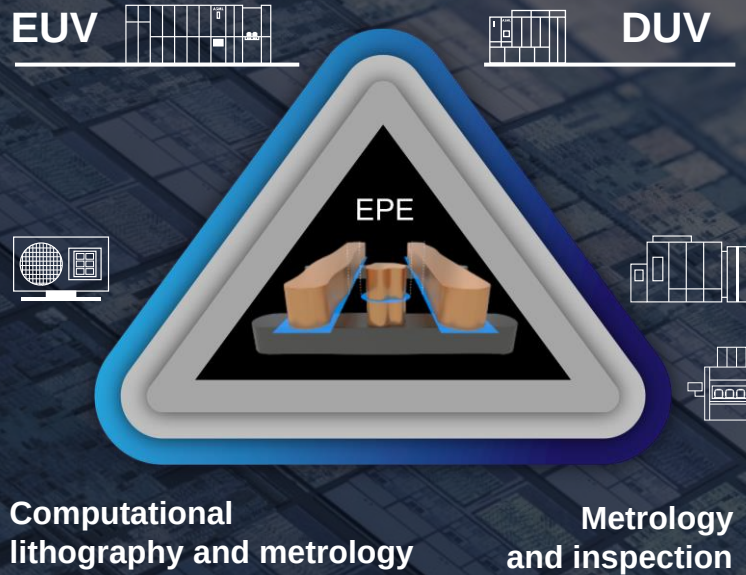
Holistic lithography process control points



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 - Followed by smaller 2D features and 3D structures requiring buried defect inspection
- **Enable** front end 3D integration (**wafer bonding**) with **metrology and control solutions** to meet customer **overlay** requirements.
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Lithography scanner
with advanced control capability



Forward Looking Statements

This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DRAM memory, statements with respect to Moore's law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for Applications products, expectations and benefits of a growing installed base, ASML's and its supplier's capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "opportunity", "scenario", "guidance," "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Moore's law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact ASML's business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law.

This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to "greenhouse gas neutral" means remaining emissions, after ASML's efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards.

An aerial, high-angle photograph of a city's street grid, showing a dense pattern of streets and blocks. The image is tilted diagonally, with the city grid running from the bottom-left towards the top-right. The colors are muted, with various shades of blue, grey, and green. The background of the entire image is a solid dark blue.

**THANK
YOU**